Retrascope - Bug #10336

Incorrect ranges in vhdl/plasma/reg_bank.vhd

05/14/2020 07:32 PM - Mikhail Lebedev

Status:	Verified	**Start date:**	05/14/2020
Priority:	Normal	**Due date:**	
Assignee:	Sergey Smolov	**% Done:**	100%
Category:	Engine (Parser)	**Estimated time:**	0.00 hour
Target version:	1.1		
Detected in build:	git	**Published in build:**	
Platform:			

Description

reg_bank design in plasma contains the following array variable:

```
type ram_type is array(31 downto 0) of std_logic_vector(31 downto 0);
variable tri_port_ram : ram_type;
```

In CFG model the data type of this variable is correct:

```
Variable[name=RAM_PROC.TRI_PORT_RAM, data=Data[type=(MAP LOGIC_INTEGER (BIT_VECTOR 32)), value=uni
nitialized]]
```

But the variable descriptor contains two ranges for it: 0:31, 0:31
This results in the following incorrect SMV-code:

```
VAR
  RAM_PROC_TRI_PORT_RAM : array 0..31 of array 0..31 of word[32];
```

One range is excessive.

Associated revisions

Revision 62674532 - 05/16/2020 12:51 PM - Sergey Smolov

vhdl-parser: fix "wrong range num" bug (#10336)

Signed-off-by: Sergey Smolov <smolov@ispras.ru>

History

#1 - 05/16/2020 12:54 PM - Sergey Smolov

- Target version set to 1.1

- Status changed from New to Resolved

- Category set to Engine (Parser)

#2 - 05/16/2020 04:13 PM - Mikhail Lebedev

- % Done changed from 0 to 100

- Status changed from Resolved to Verified

#3 - 05/16/2020 06:53 PM - Sergey Smolov

- Subject changed from Incorrect ranges in vhdl/plasma/reg_bank.vhdl to Incorrect ranges in vhdl/plasma/reg_bank.vhd