Verilog Translator - Bug #10197

Test const.v has an error.

04/01/2020 10:43 AM - Alexey Danilov

Status:	Closed	**Start date:**	04/01/2020
Priority:	Normal	**Due date:**	
Assignee:	Sergey Smolov	**% Done:**	100%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	master	**Published in build:**	0.1.3-beta-201002
Platform:			

Description

ERROR: Node 'g' has been declared two or more times

Associated revisions

Revision e90ffb7b - 04/03/2020 11:36 PM - Sergey Smolov

verilog: fix duplicate declaration (#10197)

Signed-off-by: Sergey Smolov <smolov@ispras.ru>

History

#1 - 04/01/2020 11:19 AM - Sergey Smolov

- Detected in build changed from git to master

- Assignee set to Alexander Kamkin

See const.v module, lines 9 and 12.

#2 - 04/03/2020 11:35 AM - Sergey Smolov

- Target version set to 0.1

#3 - 04/03/2020 10:05 PM - Sergey Smolov

- Assignee changed from Alexander Kamkin to Sergey Smolov

- Status changed from New to Open

#4 - 04/03/2020 11:54 PM - Sergey Smolov

- % Done changed from 0 to 100

- Status changed from Open to Resolved

#5 - 10/02/2020 02:54 PM - Sergey Smolov

- Published in build set to 0.1.3-beta-201002

- Status changed from Resolved to Closed