Verilog Translator - Bug #10141

check port redeclarations

03/03/2020 04:45 PM - Sergey Smolov

Status:	Closed	**Start date:**	03/03/2020
Priority:	Normal	**Due date:**	
Assignee:	Alexey Danilov	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	0.1		
Detected in build:	master	**Published in build:**	0.1.3-beta-201002
Platform:			

Description

IEEE-1364-2005 12.3.3

```
If a port declaration includes a net or variable type, then the port is considered completely declared, and it is
an error for the port to be declared again in a variable or net data type declaration. Because of this, all other
aspects of the port shall be declared in such a port declaration, including the signed and range definitions if
needed.
If a port declaration does not include a net or variable type, then the port can be again declared in a net or
variable declaration. If the net or variable is declared as a vector, the range specification between the two
declarations of a port shall be identical. Once a name is used in a port declaration, it shall not be declared
again in another port declaration or in a data type declaration.
```

History

#1 - 04/02/2020 04:24 PM - Alexey Danilov

- Status changed from New to Resolved

#2 - 04/19/2020 05:34 PM - Sergey Smolov

- Status changed from Resolved to Verified

#3 - 10/02/2020 02:55 PM - Sergey Smolov

- Published in build set to 0.1.3-beta-201002

- Status changed from Verified to Closed