

## Verilog Translator - Task #10009

### README\ChangeLog -> README.md\ChangeLog.md

12/24/2019 06:27 PM - Sergey Smolov

<b>Status:</b>	Closed	<b>Start date:</b>	12/24/2019
<b>Priority:</b>	Normal	<b>Due date:</b>	
<b>Assignee:</b>	Sergey Smolov	<b>% Done:</b>	100%
<b>Category:</b>		<b>Estimated time:</b>	0.00 hour
<b>Target version:</b>	0.1	<b>Published in build:</b>	0.1.3-beta-201002
<b>Detected in build:</b>	master		
<b>Description</b>			
Rewrite the specified files to Markdown format.			

#### Associated revisions

##### Revision c466e7ea - 12/24/2019 06:27 PM - Sergey Smolov

README\ChangeLog->README.md\ChangeLog.md (#10009)

Signed-off-by: Sergey Smolov <[smolov@ispras.ru](mailto:smolov@ispras.ru)>

#### History

##### #1 - 12/24/2019 06:28 PM - Sergey Smolov

- % Done changed from 0 to 100
- Status changed from New to Resolved

Done in [c466e7ea](#)

##### #2 - 12/24/2019 06:28 PM - Sergey Smolov

- Status changed from Resolved to Verified

##### #3 - 10/02/2020 02:55 PM - Sergey Smolov

- Published in build set to 0.1.3-beta-201002
- Status changed from Verified to Closed