Issues

#	Project	Tracker	Status	Priority	Subject	Author	Assignee	Target version
12607	QEMU4V	Bug	New	Normal	missing log problem	Sergey Smolov	Sergey Smolov	
12415	Trace Matcher	Task	New	Normal	use venv to build the tool	Sergey Smolov		
12282	QEMU4V	Task	New	Normal	migrate to QEMU 8.0.0	Sergey Smolov	Sergey Smolov	0.3
12249	MicroTESK for PowerPC	Bug	New	Normal	qemu-system-ppc: failed to find romfile "efi-virtio.rom"	Sergey Smolov	Sergey Smolov	
12058	QEMU4V	Task	Resolved	Normal	migrate to QEMU 7.2.0	Sergey Smolov	Sergey Smolov	0.3
12038	MicroTESK for Plasma	Developer Request	Resolved	Normal	обновление плагина PMD в Gradle	Sergey Smolov	Alexander Protsenko	
11811	QEMU4V	Task	Resolved	Normal	migrate to QEMU 7.1.0	Sergey Smolov	Sergey Smolov	0.3
11516	QEMU4V	Task	Resolved	Normal	migrate to QEMU 7.0.0	Sergey Smolov	Sergey Smolov	0.3
11042	Java SoftFloat	Bug	New	Normal	Javadoc warnings	Sergey Smolov	Alexander Protsenko	2.0
11018	Retrascope Test Suite	Task	New	Normal	Verilog duplicate removing	Sergey Smolov	Sergey Smolov	
11017	QEMU4V	Task	Resolved	Normal	migrate to QEMU 6.2.0	Sergey Smolov	Sergey Smolov	0.3
10988	Retrascope	Task	New	Normal	lowercase debug messages	Sergey Smolov	Sergey Smolov	
10888	QEMU4V	Task	Resolved	Normal	migrate to QEMU 6.1.0	Sergey Smolov	Sergey Smolov	0.3
10836	QEMU4V	Task	Resolved	Normal	migrate to QEMU 6.0.0	Sergey Smolov	Sergey Smolov	0.3
10819	MicroTESK for PowerPC	Bug	New	Normal	Trace Matcher crashes on QEMU4V empty trace	Sergey Smolov	Sergey Smolov	
10611	QEMU4V	Task	Resolved	Normal	migrate to QEMU 5.2.0	Sergey Smolov	Sergey Smolov	0.3
10513	Verilog Translator	Bug	New	Normal	macOS related line endings at Verilog modules	Sergey Smolov	Alexander Kamkin	0.1
10512	Verilog Translator	Bug	New	Normal	ADDA162H90A_atop.v line 120:47 mismatched input ':' expecting RPAREN	Sergey Smolov	Alexander Kamkin	0.1
10510	Verilog Translator	Bug	New	Normal	ERROR: [Internal] Bit vector sizes do not match: 32 != 2.	Sergey Smolov	Alexander Kamkin	0.1
10509	Verilog Translator	Bug	New	Normal	ERROR: [Internal] 0 must be > 0	Sergey Smolov	Alexander Kamkin	0.1
10508	Verilog Translator	Bug	New	Normal	ERROR: [Internal] Java heap space	Sergey Smolov	Alexander Kamkin	0.1
10505	Verilog Translator	Bug	New	Normal	ERROR: [Internal] 11 must be within range [0, 1)	Sergey Smolov	Alexander Kamkin	0.1
10502	Verilog Translator	Bug	New	Normal	subbytes.v line 76:13 no viable alternative at input '['	Sergey Smolov	Alexander Kamkin	0.1

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10494	Fortress	Task	Closed	Normal	check Windows build of Boolector on project tests	Sergey Smolov	Maxim Chudnov	0.4
10492	Fortress	Task	Closed	Normal	use CVC4 1.8 in testing	Sergey Smolov	Sergey Smolov	0.4
10474	QEMU4V	Task	Resolved	Normal	migrate to QEMU 5.1.0	Sergey Smolov	Sergey Smolov	0.3
10382	Verilog Translator	Bug	Closed	Normal	java.lang.IllegalArgumentException: expression=(BVREPEAT test.uut._saxi_maskwidth 1)	Sergey Smolov	Sergey Smolov	0.1
10370	Fortress	Bug	Closed	Normal	class ru.ispras.fortress.solver.constraint.Formulas cannot be cast to class ru.ispras.fortress.solver.constraint.Sat4jFormula	Sergey Smolov	Sergey Smolov	0.4
10304	MicroTESK	Task	New	Normal	deprecation warnings via compilation	Sergey Smolov	Alexander Kamkin	2.6
10290	Verilog Translator	Feature	New	Normal	SystemVerilog support	Sergey Smolov		
10289	Retrascope	Bug	Closed	Normal	ru.ispras.retrascope.engine.hldd.printer.smv.property.HlddPropertySmvPrinterTestCase.runTest: java.lang.OutOfMemoryError: Java heap space	Sergey Smolov	Mikhail Lebedev	1.1
10287	Retrascope	Feature	Closed	Normal	TestModel: keep top level module name & variables	Sergey Smolov	Sergey Smolov	1.1
10266	Retrascope	Bug	Closed	Normal	ru.ispras.retrascope.engine.hldd.printer.smv.HlddSmvPrinterTestCase.runTest: java.lang.NullPointerException	Sergey Smolov	Mikhail Lebedev	1.1
10258	QEMU4V	Task	Closed	Normal	migrate to QEMU 5.0	Sergey Smolov	Sergey Smolov	0.3
10246	Verilog Translator	Bug	Rejected	Normal	ru.ispras.verilog.parser.VerilogQuipTestSuite#runTest_nut_001: ERROR: Module 'lut_output' has not been found	Sergey Smolov	Alexander Kamkin	0.1
10245	Verilog Translator	Bug	Closed	Normal	ru.ispras.verilog.parser.VerilogQuipTestSuite#runTest_pci_wbw_wbr_fifos: ERROR: [Internal] null	Sergey Smolov	Alexey Danilov	0.1
10241	Verilog Translator	Bug	Closed	Normal	ru.ispras.verilog.parser.VerilogQuipTestSuite#runTest_dctub_jpeg: ERROR: ..\src\test\verilog\hdl-benchmarks\hdl\quip\oc_video_compression_systems_jpeg\dct_cos_table.v line 1:70 mismatched character '\r' expecting '\n'	Sergey Smolov	Alexander Kamkin	0.1
10238	Retrascope	Feature	Closed	Normal	VerilogParser: '--library-file' cmdline option	Sergey Smolov	Sergey Smolov	1.1
10237	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.VerilogTexas97TestSuite#runTest_Pi_Bus_single_master_main2: ERROR: Cycle inclusion at: '...bus.v'	Sergey Smolov	Alexey Danilov	0.1
10236	Retrascope	Bug	Rejected	Normal	efsm-test-generator hangs at opencores/mips16/data_mem.v	Sergey Smolov	Sergey Smolov	1.1
10216	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.VerilogQuipTestSuite#runTest_nut_001: java.lang.NullPointerException	Sergey Smolov	Alexey Danilov	0.1
10215	Verilog Translator	Bug	New	Normal	ERROR: Starting points limit has been exhausted: 2255	Sergey Smolov	Alexander Kamkin	0.1
10214	Verilog Translator	Bug	Rejected	Normal	ru.ispras.verilog.parser.VerilogQuipTestSuite#runTest_nut_000: nut_000_lut.v line 7:0 no viable alternative at input 'module'	Sergey Smolov	Sergey Smolov	0.1
10202	Verilog Translator	Bug	Closed	Normal	SVA grammar warnings via assembling	Sergey Smolov	Mikhail Lebedev	0.1
10191	Retrascope	Bug	Closed	Normal	java.lang.IllegalArgumentException: Specified target vertex 0 is not part of graph	Sergey Smolov	Sergey Smolov	1.1
10174	Retrascope	Bug	Closed	High	nondeterminism at EFSM transitions generation	Sergey Smolov	Sergey Smolov	1.1

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10173	Verilog Translator	Bug	Closed	High	javadoc: DefineStructure.java:37: warning: no @return	Sergey Smolov	Alexey Danilov	0.1
10166	Retrascope	Task	Closed	Normal	rename some class fields & related methods	Sergey Smolov	Sergey Smolov	1.1
10141	Verilog Translator	Bug	Closed	Normal	check port redeclarations	Sergey Smolov	Alexey Danilov	0.1
10139	Retrascope	Task	Closed	High	fix coding issues at *BenchTest classes	Sergey Smolov	Maxim Chudnov	1.1
10133	Retrascope	Task	New	Normal	use '-coi' model checker option	Sergey Smolov	Mikhail Lebedev	1.1
10131	Verilog Translator	Bug	Closed	Normal	ru.ispras.verilog.parser.VerilogIwlsTestCase.runTest_iscas_s9234_1: java.lang.OutOfMemoryError: Java heap space	Sergey Smolov	Alexander Kamkin	0.1
10128	Retrascope	Task	Closed	Normal	rename multi-test classes: "*TestCase" -> "*TestSuite"	Sergey Smolov	Maxim Chudnov	1.1
10125	Retrascope	Feature	Closed	Normal	'--detailed' option for efsm-graphml-printer engine	Sergey Smolov	Sergey Smolov	1.1
10121	MicroTESK	Bug	Open	Normal	technical output printing at 'compile.sh' script running with '--help' option	Sergey Smolov	Alexander Kamkin	2.6
10116	Retrascope	Feature	Closed	Normal	command line option to check if solvers\model checkers that are used are installed properly	Sergey Smolov	Sergey Smolov	1.1
10115	Retrascope	Feature	Closed	Normal	'--version' command line option	Sergey Smolov	Sergey Smolov	1.1
10112	Retrascope	Feature	Closed	Normal	'--no-phase' command line option for 'cfg-gadd-transformer' engine	Sergey Smolov	Sergey Smolov	1.1
10102	MicroTESK	Bug	Closed	High	incorrect ld scripts for x86 test programs	Sergey Smolov	Alexander Kamkin	2.5
10100	Trace Matcher	Feature	Resolved	Normal	"--boot-size <num>" command line option	Sergey Smolov	Sergey Smolov	0.1
10099	Trace Matcher	Feature	Resolved	Normal	"--start-addr <hex value>" command line option	Sergey Smolov	Sergey Smolov	0.1
10094	MicroTESK	Bug	Closed	Normal	strange common code at LinkerScript.stg	Sergey Smolov	Alexander Kamkin	2.5
10088	QEMU4V	Feature	New	Low	QEMU4V formatted traces for x86 programs	Sergey Smolov		
10085	Retrascope	Bug	Closed	Normal	EfsmTransitionPropertyExtractorTestCase: There is no declaration of variable neither in this EFSM nor in its ancestors: process_0.D	Sergey Smolov	Sergey Smolov	1.1
10082	Retrascope	Bug	New	Normal	WARNING: Illegal reflective access by org.python.core.PySystemState	Sergey Smolov	Sergey Smolov	1.1
10081	Retrascope	Bug	Closed	High	tool hangs right after final "Duration: " msg	Sergey Smolov	Sergey Smolov	1.1
10075	Retrascope	Bug	Closed	Normal	jython.jar: WARNING: An illegal reflective access operation has occurred at JDK 11	Sergey Smolov	Sergey Smolov	1.1
10074	MicroTESK	Feature	New	Normal	option that stores boot obj at the generated ld script	Sergey Smolov	Alexander Kamkin	2.6
10073	Retrascope	Task	Closed	High	fix checkstyle warnings	Sergey Smolov	Maxim Chudnov	1.1
10069	MicroTESK	Bug	New	Normal	cpu.nml Error: Internal error: context [/Isa] 1:8 attribute file isn't defined	Sergey Smolov	Alexander Kamkin	2.6
10060	Retrascope	Feature	Closed	High	Support SVA properties in CFG model	Sergey Smolov	Sergey Smolov	1.2
10059	Retrascope	Task	Rejected	Normal	mv all the project tests to JUnit 5 platform	Sergey Smolov	Maxim Chudnov	1.1

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10058	Retrascope	Task	New	Normal	User documentation	Sergey Smolov	Sergey Smolov	1.2
10041	QEMU4V	Bug	Closed	Normal	wrong names for PowerPC registers in trace	Sergey Smolov	Sergey Smolov	0.3
10031	MicroTESK for PowerPC	Bug	New	Normal	WARNING: An illegal reflective access operation has occurred	Sergey Smolov	Alexander Protsenko	0.0
10023	Retrascope	Bug	Closed	High	ru.ispras.retrascope.parser.verilog.VerilogParserTestCase: java.lang.Exception: Method runTest should have no parameters	Sergey Smolov	Maxim Chudnov	1.1
10018	Trace Matcher	Task	Closed	Normal	migrate to Python 3	Sergey Smolov	Sergey Smolov	0.1
10017	Trace Matcher	Task	Closed	Normal	README\ChangeLog -> README.md\ChangeLog.md	Sergey Smolov	Sergey Smolov	0.1
10016	Trace Matcher	Task	Closed	Normal	Use Gradle 4.10.3 in build system	Sergey Smolov	Sergey Smolov	0.1
10015	Trace Matcher	Feature	Closed	Normal	Report an error when input file is empty	Sergey Smolov	Sergey Smolov	0.1
10009	Verilog Translator	Task	Closed	Normal	README\ChangeLog -> README.md\ChangeLog.md	Sergey Smolov	Sergey Smolov	0.1
10002	Fortress	Task	Closed	Normal	get Boolector solver from server as dependency	Sergey Smolov	Sergey Smolov	0.4
10001	Fortress	Task	Rejected	Normal	SMT-LIBv2 benchmarks	Sergey Smolov		
10000	Retrascope	Task	Closed	Normal	README\ChangeLog -> README.md\ChangeLog.md	Sergey Smolov	Sergey Smolov	1.1
9999	Castle	Task	Closed	Normal	ChangeLog -> ChangeLog.md	Sergey Smolov	Sergey Smolov	0.1
9998	Castle	Task	Closed	Normal	README -> README.md	Sergey Smolov	Sergey Smolov	0.1
9993	Verilog Translator	Bug	New	High	if two modules are passed to the tool and one includes another, the tool hangs	Sergey Smolov	Alexander Kamkin	0.1
9990	Verilog Translator	Feature	Closed	High	check for variable/net redeclarations	Sergey Smolov	Alexey Danilov	0.1
9986	QEMU4V	Task	New	Normal	check if QEMU4V features can be implemented as TCG plugin	Sergey Smolov	Sergey Smolov	0.3
9971	MicroTESK for RISC-V	Task	Closed	Normal	print Spike trace to separate log file for every JUnit test case	Sergey Smolov	Sergey Smolov	0.1
9964	Retrascope	Task	Closed	Normal	add HDL examples to project distribution	Sergey Smolov	Sergey Smolov	1.1
9962	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.sample.Mips16CoreTopTestCase: java.lang.IllegalArgumentException	Sergey Smolov	Alexey Danilov	0.1
9936	Verilog Translator	Bug	Closed	High	tabs in "`define" directive cause java.lang.NumberFormatException	Sergey Smolov	Alexey Danilov	0.1
9917	QEMU4V	Task	Closed	Normal	check QEMU4V-specific code on compliance with coding style	Sergey Smolov	Sergey Smolov	0.3
9915	Verilog Translator	Bug	Closed	Urgent	"Cycle inclusion has been detected in fine <filename>" error is reported for Verilog modules that use the same another file	Sergey Smolov	Alexey Danilov	0.1
9911	Retrascope	Task	Closed	Urgent	merge "*/sample/*TestCase" Java test cases	Sergey Smolov	Maxim Chudnov	1.1
9909	QEMU4V	Task	Closed	Normal	migrate to QEMU 4.2.0	Sergey Smolov	Sergey Smolov	0.3
9904	Verilog Translator	Task	Closed	Normal	add info for "--library-file" cmdline option	Sergey Smolov	Alexander Kamkin	0.1

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9902	Verilog Translator	Bug	New	High	java.lang.IllegalArgumentException: Descriptor for '<var name>' has not been found	Sergey Smolov	Alexander Kamkin	0.1
9901	Retrascope Test Suite	Bug	New	Low	initializationError in some tests after Jenkins update	Sergey Smolov	Mikhail Lebedev	
9899	Verilog Translator	Task	Closed	Normal	VerilogPrinter test cases for QUIP benchmarks	Sergey Smolov	Maxim Chudnov	0.1
9892	MicroTESK for RISC-V	Bug	Closed	Normal	WARNING: An illegal reflective access operation has occurred	Sergey Smolov	Alexander Protsenko	0.1
9889	MicroTESK for Plasma	Task	Resolved	Normal	rm deprecated 'findbugs' plugin from Gradle build script	Sergey Smolov		
9888	Retrascope IDE	Task	New	Normal	complete migration from Ant to Gradle build system	Sergey Smolov		0.1
9863	QEMU4V	Task	Closed	Normal	use Gradle 4.10.3	Sergey Smolov	Sergey Smolov	0.3
9862	QEMU4V	Task	Closed	Normal	migrate to QEMU 4.1.0	Sergey Smolov	Sergey Smolov	0.3
9859	Verilog Translator	Task	New	Normal	modify "ERROR: [Internal] null" line at error log	Sergey Smolov	Alexander Kamkin	0.1
9848	Verilog Translator	Bug	Closed	Normal	ru.ispras.verilog.parser.VerilogVisVerilog2SmvTestCase.runTest_Pci_Bus_Verilog_Mv_files_PciNorm: Function declaration '$ND' has not been found	Sergey Smolov	Sergey Smolov	0.1
9844	Retrascope Test Suite	Bug	Rejected	Normal	Bash scripts that run side tools (EBMC, SymbiYosys, Verilog2SMV) can't extract names of several Verilog modules	Sergey Smolov	Sergey Smolov	
9839	Retrascope Test Suite	Task	Rejected	Normal	scripts for commercial FV tools running	Sergey Smolov	Sergey Smolov	
9823	Retrascope IDE	Task	Verified	Normal	README.txt -> README	Sergey Smolov	Maxim Chudnov	0.1
9822	Verilog Translator	Bug	Closed	Normal	ru.ispras.verilog.parser.VerilogIeeeTestCase.runTest_10_04_04_1: Starting points limit has been exhausted: 513	Sergey Smolov	Sergey Smolov	0.1
9816	Retrascope IDE	Bug	New	Normal	Retrascope IDE does not appear in "Installed Software" menu	Sergey Smolov		0.1
9815	Retrascope IDE	Task	New	Normal	uninstaller for Retrascope IDE	Sergey Smolov		0.1
9811	Verilog Translator	Task	Closed	High	macro with parameters	Sergey Smolov	Alexey Danilov	0.2
9810	Retrascope IDE	Task	New	Normal	Gradle build system	Sergey Smolov		0.1
9806	Retrascope	Task	Closed	Normal	rm dependency from commons-lang library	Sergey Smolov	Sergey Smolov	1.0
9803	Verilog Translator	Bug	Closed	Normal	ru.ispras.verilog.parser.sample.MulFifoTestCase: NullPointerException at ru.ispras.verilog.parser.elaborator.VerilogElaborator$1.getNode(VerilogElaborator.java:932)	Sergey Smolov	Alexander Kamkin	0.1
9802	Verilog Translator	Bug	Closed	Normal	ru.ispras.verilog.parser.sample.FuncTestCase: NullPointerException at ru.ispras.verilog.parser.elaborator.VerilogElaborator.createVariableAndBinding(VerilogElaborator.java:512)	Sergey Smolov	Alexander Kamkin	0.1
9798	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.sample.Bug9798TestCase: incorrect BVEXTRACT params for bit vector variable with offset	Sergey Smolov	Alexander Kamkin	0.1

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9790	Verilog Translator	Task	New	Normal	external names for unnamed generate blocks	Sergey Smolov	Alexander Kamkin	0.1
9784	Verilog Translator	Bug	Closed	Normal	mul_fifo.v: wrong Fortress-based node representation of assignment left-hand side	Sergey Smolov	Sergey Smolov	0.1
9776	Retrascope IDE	Task	Verified	Normal	try to use SVEditor instead of veditor	Sergey Smolov	Maxim Chudnov	0.1
9775	Verilog Translator	Bug	Closed	Normal	ru.ispras.verilog.parser.VerilogIeeeTestCase.runTest_10_04_04_1: Conversion = "'	Sergey Smolov	Alexander Kamkin	0.1
9773	Verilog Translator	Bug	Rejected	Normal	ru.ispras.verilog.parser.VerilogIeeeTestCase.runTest_10_04_03_1: ru.ispras.fortress.expression.NodeOperation cannot be cast to ru.ispras.fortress.expression.NodeValue	Sergey Smolov	Alexander Kamkin	0.1
9771	Verilog Translator	Task	Closed	Normal	fix 'publishing' block behaviour for Gradle 4.10.3	Sergey Smolov	Sergey Smolov	0.1
9769	Retrascope	Feature	Closed	Normal	GraphML printers: make branch values italic	Sergey Smolov	Sergey Smolov	1.0
9767	Retrascope	Feature	Closed	Normal	GraphML printers: use dotted arrows for Module->(Module| Process) hierarchy dependencies	Sergey Smolov	Sergey Smolov	1.0
9766	Retrascope	Task	Closed	High	remove 'vhdl.record' Git branch from remote repo	Sergey Smolov	Maxim Chudnov	1.0
9764	Retrascope IDE	Task	New	High	migrate to Eclipse 2019	Sergey Smolov		0.1
9763	Retrascope Test Suite	Bug	Closed	Normal	missing javadoc headers in Java files of 'ru.ispras.retrascope.engine.hldd.printer.smv.spec.sample.vcegar' package	Sergey Smolov	Mikhail Lebedev	
9762	Retrascope	Task	Closed	High	prepare to 1.1.1 release	Sergey Smolov	Sergey Smolov	1.0
9726	Retrascope Test Suite	Task	Closed	Normal	VerilogPrinter test cases	Sergey Smolov	Sergey Smolov	
9670	Retrascope Test Suite	Task	New	High	add 'ar.v' module to the test suite when SVA support will be implemented	Sergey Smolov	Sergey Smolov	
9658	Retrascope	Task	Closed	Normal	Check for duplicated data access conflict assertions	Sergey Smolov	Mikhail Lebedev	1.0
9607	Retrascope Test Suite	Task	Closed	Normal	add QUIP 9.0 benchmark	Sergey Smolov	Sergey Smolov	
9606	Retrascope Test Suite	Task	Closed	Normal	add IWLS 2005 benchmark	Sergey Smolov	Sergey Smolov	
9594	Verilog Translator	Bug	Closed	Normal	extra 'BVEXTRACT' operation in right hand side expression in 'assign' block's statement	Sergey Smolov	Alexander Kamkin	0.1
9566	Retrascope Test Suite	Task	Closed	Normal	tests for Yosys-SMTBMC tool	Sergey Smolov	Sergey Smolov	
9565	Retrascope Test Suite	Task	Closed	Normal	tests for Verilog2SMV tool	Sergey Smolov	Sergey Smolov	
9564	Retrascope Test Suite	Task	Closed	Normal	tests for EBMC tool	Sergey Smolov	Sergey Smolov	
9562	Retrascope	Bug	Closed	Normal	ru.ispras.retrascope.engine.hldd.printer.smv.usedef.MemStageUseDefSmvPrinterTestCase: model checker crashes without errors in *.smvlog	Sergey Smolov	Mikhail Lebedev	1.0

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9521	Retrascope	Bug	Closed	High	NuSMV works too slow on ITC'99 b11 design	Sergey Smolov	Mikhail Lebedev	1.0
9503	Retrascope	Feature	Closed	Normal	when debug option is enabled, pass it to the model checker as well	Sergey Smolov	Mikhail Lebedev	1.0
9488	Retrascope	Task	New	Normal	CFG-GADD transformer backend that makes assignments index and range-free	Sergey Smolov	Sergey Smolov	1.2
9486	Retrascope	Feature	Closed	Normal	HDL parser's init_process backend: calculate initial values if possible	Sergey Smolov	Sergey Smolov	1.0
9485	Retrascope	Bug	Closed	Normal	missing javadoc	Sergey Smolov	Mikhail Lebedev	1.0
9484	Retrascope	Task	Closed	Normal	Check variables\switches\basic blocks number at HDL parser test cases	Sergey Smolov	Sergey Smolov	1.0
9482	Retrascope RISC-V Benchmark	Bug	Closed	Normal	ru.ispras.retrascope.sample.VexRiscvVexRiscvGaddTestCase: ERROR: Wrong number of out edges for 'ru.ispras.retrascope.model.cfg.CfgBlockStatement@c219bf5': 2	Sergey Smolov	Sergey Smolov	
9478	Retrascope RISC-V Benchmark	Bug	New	Normal	ERROR: retrascope-riscv\src\main\verilog\rocket-chip\src\main\resources\vsrc\TestDriver.v line 28:2 no viable alternative at input 'int'	Sergey Smolov		
9477	Retrascope RISC-V Benchmark	Bug	New	Normal	an "import "DPI-C" function" construction causes Verilog Translator error	Sergey Smolov	Alexander Kamkin	
9475	Retrascope RISC-V Benchmark	Bug	Closed	Normal	Picorv32Hx8kdemoVerilogPrinterTestCase: ERROR: line 1:0 no viable alternative at input '('	Sergey Smolov	Alexander Kamkin	
9474	Retrascope	Feature	Closed	Normal	enable\disable backend parameters for all the engines	Sergey Smolov	Sergey Smolov	1.0
9468	Retrascope	Feature	Closed	Normal	HDL parser backend that removes 'initial' processes	Sergey Smolov	Sergey Smolov	1.0
9463	Retrascope	Bug	Closed	Normal	check if jUnit test cases for CfgCgaaTransformer return same results on different machines\platforms	Sergey Smolov	Sergey Smolov	1.0
9462	Retrascope	Task	Closed	Normal	jUnit test cases for HDL parsers that count numbers of CFG processes, statements, etc.	Sergey Smolov	Sergey Smolov	1.0
9457	Retrascope	Feature	Closed	Normal	one more auxiliary path in GADD model for terminal endings	Sergey Smolov	Sergey Smolov	1.0
9446	Retrascope	Feature	Closed	Normal	Debug output file for engines and their backends	Sergey Smolov	Sergey Smolov	1.0
9438	Retrascope	Task	Closed	Normal	jUnit test cases for CFG-GAD transformer that check path number	Sergey Smolov	Sergey Smolov	1.0
9437	MicroTESK	Bug	Closed	Normal	ru.ispras.microtesk.model.minimips.BufferPreparatorTestCase: QEMU4V crashes with general protection error on this test program	Sergey Smolov	Sergey Smolov	2.4
9436	MicroTESK	Bug	Closed	Normal	ru.ispras.microtesk.mmu.translator.GeneralTestCase: java.lang.IllegalArgumentException	Sergey Smolov	Alexander Kamkin	2.5
9430	Retrascope	Task	Closed	Normal	CGAA -> GADD	Sergey Smolov	Sergey Smolov	1.0
9427	Retrascope	Task	Closed	Normal	reuse variables' versions upon CGAA model building	Sergey Smolov	Sergey Smolov	1.0
9415	QEMU4V	Task	Closed	Normal	migrate to QEMU 3.1.0	Sergey Smolov	Sergey Smolov	0.3
9389	Retrascope	Task	Closed	Normal	Assertion -> Property	Sergey Smolov	Sergey Smolov	1.0

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9387	MicroTESK for PowerPC	Bug	Closed	Normal	ru.ispras.microtesk.model.powerpc.InstructionBPUTestCase: ../microtesk-powerpc/build/test/instruction_bpu/instruction_bpu_0000.s:47: Error: operand out of range (0x0000000000002774 is not between 0x0000000000000000 and 0x000000000000001	Sergey Smolov	Alexander Protsenko	
9386	MicroTESK for PowerPC	Bug	Closed	High	ru.ispras.microtesk.model.powerpc.InstructionALUTestCase: Assembler messages: ../microtesk-powerpc/build/test/instruction_alu/instruction_alu_0000.s:1: Error: junk at end of line, first unrecognized character is `/'	Sergey Smolov	Sergey Smolov	
9377	MicroTESK for MIPS	Bug	New	Normal	'Failed to construct decoder' warnings in project's build log	Sergey Smolov	Alexander Kamkin	
9376	MicroTESK for MIPS	Bug	New	Normal	Warning: Group MIPS64FpuOp contains two items add_fmt and mfc1 with the same opcode 01000100000000000000000000000000	Sergey Smolov	Alexander Kamkin	
9375	MicroTESK for PowerPC	Bug	Closed	Normal	ru.ispras.microtesk.model.powerpc.autogen.GroupTestCase: org.jruby.exceptions.RaiseException: (NoMethodError) undefined method `la' for #<GroupGenTemplate:0x6046f0da>	Sergey Smolov	Alexander Protsenko	
9374	MicroTESK for PowerPC	Bug	Closed	Normal	ru.ispras.microtesk.model.powerpc.autogen.BoundaryTestCase: Simulation failedThe CPR storage is not defined in the model.ru.ispras.microtesk.model.ConfigurationException: The CPR storage is not defined in the model.	Sergey Smolov	Alexander Protsenko	
9373	QEMU4V	Task	Closed	Normal	write a PowerPC-related chapter to "Getting Started"	Sergey Smolov	Maxim Chudnov	0.3
9365	QEMU4V	Bug	Closed	Normal	missing insn binary images in MIPS trace	Sergey Smolov	Sergey Smolov	0.2
9363	QEMU4V	Task	Closed	Normal	remove 'set_q4v_tstamp' function calls from RISC-V/MIPS/Aarch64 'cpu_loop.c' modules	Sergey Smolov	Sergey Smolov	0.2
9335	Retrascope	Feature	Closed	Normal	cgaa-assert-extractor engine	Sergey Smolov	Mikhail Lebedev	1.0
9334	QEMU4V	Bug	Closed	Normal	timestamp reset at MIPS trace	Sergey Smolov	Sergey Smolov	0.2
9333	QEMU4V	Bug	Closed	Normal	unexpected hex value in MIPS trace	Sergey Smolov	Sergey Smolov	0.2
9311	Verilog Translator	Task	Closed	High	type casting of expression operands	Sergey Smolov	Sergey Smolov	0.1
9310	Retrascope	Task	Closed	Normal	substitute SMT-LIB variables those names are equal to builtin commands	Sergey Smolov	Sergey Smolov	1.0
9309	Retrascope Test Suite	Bug	Closed	Normal	ru.ispras.retrascope.engine.smv.testbench.sample.vcegar.VcegarPiBusAssertSmvTestbench TestCase:line 2 column 34: invalid declaration, builtin symbol select	Sergey Smolov	Sergey Smolov	
9296	Verilog Translator	Bug	Closed	High	vcegar-tests/cache_coherence/two_processor_bin_2.v:46: illegal types of "then" and "else" expressions : unsigned word[1] and boolean	Sergey Smolov	Alexander Kamkin	0.1
9291	Retrascope	Task	Closed	Normal	use nuXmv 1.1.1	Sergey Smolov	Sergey Smolov	1.0
9288	QEMU4V	Bug	Closed	Immediate	/target/mips/translate.c:2617:9: error: ‘else’ without a previous ‘if’	Sergey Smolov	Maxim Chudnov	0.2
9282	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.sample.DataMemTestCase: DEBUG: Reduce: (BVEXTRACT 0 7 mem_access_addr)	Sergey Smolov	Alexander Kamkin	0.1
9281	Retrascope	Feature	Closed	Normal	cmdline option that specifies clock variable for CGAA model	Sergey Smolov	Sergey Smolov	1.0
9280	Retrascope	Task	Closed	Normal	prepare the code to 1.1.1 release	Sergey Smolov	Mikhail Lebedev	1.0
9278	Retrascope	Task	Closed	Normal	use CGAA model instead of EFSM-based assertions to get clocks	Sergey Smolov	Mikhail Lebedev	1.0
9277	Retrascope	Task	Closed	High	mv clock-like variable detection to CFG-to-CGAA transformer	Sergey Smolov	Sergey Smolov	1.0

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9276	Verilog Translator	Bug	Rejected	Normal	no errors returned for bug-with-macro-containing module	Sergey Smolov	Alexander Kamkin	0.1
9269	QEMU4V	Task	Closed	Normal	migrate to QEMU 3.0.0	Sergey Smolov	Sergey Smolov	0.2
9264	Retrascope	Feature	Closed	Normal	'--disable-backends' cmdline option for HDL parser engine	Sergey Smolov	Sergey Smolov	1.0
9251	Verilog Translator	Task	Closed	High	calculate type of index for bit-vector arrays	Sergey Smolov	Alexander Kamkin	0.1
9250	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.sample.IfStageTestCase: src/test/verilog/rest-tests/mips16/IF_stage.v line 31:9 missing KW_BEGIN at 'pc'	Sergey Smolov	Alexander Kamkin	0.1
9249	Retrascope	Task	Closed	Normal	separate jUnit test cases for EfsmGraphMlPrinter engine	Sergey Smolov	Sergey Smolov	1.0
9248	Retrascope	Task	Closed	High	CFG model process should not have it's own internal variables	Sergey Smolov	Sergey Smolov	1.0
9247	Retrascope	Feature	Open	High	CFG-to-C printer	Sergey Smolov	Sergey Smolov	1.2
9242	Retrascope	Task	Closed	High	check BVEXTRACT operation's parameter order	Sergey Smolov	Sergey Smolov	1.0
9239	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.sample.Mips16CoreTopTestCase: java.lang.IllegalArgumentException	Sergey Smolov	Alexander Kamkin	0.1
9235	Retrascope Test Suite	Task	Closed	Normal	adapt JUnit components to new interface of ToolTest class	Sergey Smolov	Mikhail Lebedev	
9232	Verilog Translator	Task	Closed	High	remove typedefs from texas97-tests/PPC60X_bus/src/define.v	Sergey Smolov	Mikhail Lebedev	0.1
9231	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.VerilogTexas97TestCase.runTest_PI_BUS_single_master_master2: java.lang.NullPointerException	Sergey Smolov	Sergey Smolov	0.1
9230	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.VerilogTexas97TestCase.runTest_PI_BUS_multi_master_bus: java.lang.IllegalArgumentException	Sergey Smolov	Sergey Smolov	0.1
9227	Retrascope	Feature	Closed	High	support for 'BVEXTRACT(x y (SELECT z w))' constructions in left hand sides of assigments	Sergey Smolov	Sergey Smolov	1.0
9226	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.VerilogVcegarTestCase.runTest_small_pipeline_pipeline_smv: /src/test/verilog/vcegar-tests/small/pipeline/pipeline_smv.v line 38:10 no viable alternative at input 'property'	Sergey Smolov	Mikhail Lebedev	0.1
9225	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.VerilogTexas97TestCase.runTest_MPEG_prefixcode: ERROR: ../texas97-tests/MPEG/prefixcode.v line 70:8 no viable alternative at input ';'	Sergey Smolov	Mikhail Lebedev	0.1
9224	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.VerilogTexas97TestCase.runTest_PCI_BUS_Verilog_MV_files_PCInorm: ERROR: Function declaration '$random' has not been found	Sergey Smolov	Alexander Kamkin	0.1
9223	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.VerilogVcegarTestCase.runTest_pj_icu_icctl1: ERROR: Declaration of 'clk' has not been found	Sergey Smolov	Mikhail Lebedev	0.1
9222	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.VerilogVisVerilog2SmvTestCase.runTest_Sampleq_twoFifo1: java.lang.IllegalStateException: Parameter is not a value: LOGLENGTH	Sergey Smolov	Alexander Kamkin	0.1
9217	MicroTESK	Task	Closed	Normal	Use 'ru.ispras.castle.codegen' package classes from Castle	Sergey Smolov		
9216	Retrascope Test Suite	Task	Closed	Normal	remove tests for Verilog Translator from project	Sergey Smolov	Mikhail Lebedev	

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9215	Verilog Translator	Bug	Rejected	High	ru.ispras.verilog.parser.VerilogTexas97TestCase.runTest_PPC60X_bus_src_mem: Module 'AddrStatus' cannot be found	Sergey Smolov	Alexander Kamkin	0.1
9214	Verilog Translator	Bug	Rejected	High	ru.ispras.verilog.parser.VerilogTexas97TestCase.runTest_PPC60X_bus_src_cpu: Module 'AddressTenure' cannot be found	Sergey Smolov	Alexander Kamkin	0.1
9213	Verilog Translator	Bug	Rejected	High	ru.ispras.verilog.parser.VerilogTexas97TestCase.runTest_PPC60X_bus_src_arbiter: Module 'ArbiterStatus' cannot be found	Sergey Smolov	Alexander Kamkin	0.1
9212	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.VerilogVisVerilog2SmvTestCase.runTest_Vlunc_vlunc: Module 'transform' cannot be found	Sergey Smolov	Alexander Kamkin	0.1
9211	Verilog Translator	Bug	Closed	High	java.lang.IllegalArgumentException at ru.ispras.verilog.parser.model.VerilogModule.addDeclaration(VerilogModule.java:193)	Sergey Smolov	Alexander Kamkin	0.1
9210	Verilog Translator	Bug	Closed	High	java.lang.IllegalArgumentException at ru.ispras.fortress.expression.Nodes.bvextract(Nodes.java:322)	Sergey Smolov	Alexander Kamkin	0.1
9209	Verilog Translator	Bug	Closed	High	java.util.EmptyStackException at ru.ispras.verilog.parser.util.TokenSourceStack.getLastParentToken(TokenSourceStack.java:70)	Sergey Smolov	Sergey Smolov	0.1
9208	Verilog Translator	Task	Closed	Normal	add Verilog2Smv\VIS benchmark to project test suite	Sergey Smolov	Sergey Smolov	0.1
9207	Verilog Translator	Task	Closed	Normal	add VCEGAR benchmark to project test suite	Sergey Smolov	Sergey Smolov	0.1
9206	Verilog Translator	Task	Closed	Normal	add Texas97 benchmark to project test suite	Sergey Smolov	Sergey Smolov	0.1
9203	Retrascope Test Suite	Bug	Closed	Normal	ru.ispras.retrascope.basis.HlddAssertSmvTestbenchBenchmarkTest.runTest: java.lang.IllegalArgumentException: 'benchmarks' field is not initialized.	Sergey Smolov	Mikhail Lebedev	
9202	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.sample.PjIcuIcctl1TestCase: java.lang.ArrayIndexOutOfBoundsException: 3	Sergey Smolov	Alexander Kamkin	0.1
9196	Retrascope	Task	Closed	Normal	CfgVarRangeBlockBackend: use array length for assignment elaboration	Sergey Smolov	Sergey Smolov	1.0
9191	Retrascope	Task	Closed	Normal	use StringTemplate facilities to generate HDL testbenches	Sergey Smolov	Sergey Smolov	1.0
9190	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.sample.DescriptorBuffersTestCase: incorrect calculation for string parameter values	Sergey Smolov	Alexander Kamkin	0.1
9184	Veritool	Bug	New	Normal	ERROR: Unable to read config file: /usr/lib/x86_64-linux-gnu/ivl/veritool.conf	Sergey Smolov		
9182	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.sample.MulFifoTestCase: java.lang.IllegalStateException: Parameter is not a value: i	Sergey Smolov	Alexander Kamkin	0.1
9176	Retrascope Test Suite	Bug	Closed	Normal	VcegarHlddSmvPrinterTestCase: java.lang.IllegalArgumentException: Unknown operation 'BVSDIV'	Sergey Smolov	Mikhail Lebedev	
9175	Retrascope Test Suite	Bug	Closed	Normal	Texas97PdlxCfgGraphMlTestCase: NullPointerException	Sergey Smolov	Sergey Smolov	
9174	Verilog Translator	Bug	Closed	High	NullPointerException via VerilogLiteral construction	Sergey Smolov	Alexander Kamkin	0.1

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9173	Verilog Translator	Bug	Closed	High	Incorrect DataType: BIT_VECTOR(1) instead of BIT_VECTOR(40)	Sergey Smolov	Alexander Kamkin	0.1
9172	Retrascope Test Suite	Bug	Closed	Normal	Texas97ParsepackCfgGraphMlTestCase: ru.ispras.retrascope.basis.exception.RetrascopeException: Wrong range: 0 < 0 or 7 > 1.	Sergey Smolov	Sergey Smolov	
9165	Verilog Translator	Bug	Closed	High	Incorrect parameter value calculation at hierarchical Verilog description	Sergey Smolov	Alexander Kamkin	0.1
9160	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.sample.Mips16CoreTopTestCase: Module 'mips_16_core_top' cannot be found	Sergey Smolov	Alexander Kamkin	0.1
9149	Retrascope	Feature	Closed	Normal	elaborate ranged assignments for bitvector target variables	Sergey Smolov	Sergey Smolov	1.0
9123	Fortress	Feature	Closed	High	calculate DataType for 'BVEXTRACT(i, i, x)' NodeOperation objects	Sergey Smolov	Sergey Smolov	0.4
9079	QEMU4V	Feature	Closed	Normal	basic support for MIPS32	Sergey Smolov	Sergey Smolov	0.2
9075	Retrascope	Bug	Closed	Normal	java.lang.IllegalArgumentException: testNum 0 != 1 topModuleNum	Sergey Smolov	Sergey Smolov	1.0
9071	Retrascope Test Suite	Bug	Open	Normal	ru.ispras.retrascope.engine.hldd.printer.smv.Texas97HlddSmvPrinterTestCase.runTest: java.lang.IllegalArgumentException: Unknown operation 'FUNCTION'	Sergey Smolov	Mikhail Lebedev	
9066	Retrascope	Bug	Closed	Normal	ru.ispras.retrascope.engine.hldd.printer.smv.Texas97HlddSmvPrinterTestCase.runTest: java.lang.NullPointerException	Sergey Smolov	Sergey Smolov	1.0
9063	MicroTESK	Bug	Closed	Normal	microtesk/src/main/java/core/ru/ispras/microtesk/utils/PropertyMap.java uses unchecked or unsafe operations	Sergey Smolov	Alexander Kamkin	2.5
9055	Verilog Translator	Bug	Closed	High	Texas97IFetchVerilogPrinterTestCase: java.lang.IndexOutOfBoundsException: 4294967283 is out of bounds.	Sergey Smolov	Alexander Kamkin	0.1
9051	QEMU4V	Feature	Closed	Normal	basic support for PowerPC emulation	Sergey Smolov	Sergey Smolov	0.3
9050	QEMU4V	Feature	Closed	Normal	basic support for i386 emulation	Sergey Smolov	Sergey Smolov	
9049	QEMU4V	Feature	Closed	Normal	basic support for MIPS64 emulation	Sergey Smolov	Sergey Smolov	0.2
9041	Retrascope	Feature	Closed	Normal	when model checker returns an error, print it's log to the Retrascope output	Sergey Smolov	Mikhail Lebedev	1.0
9039	Retrascope	Feature	Closed	Normal	Support for designs that assign to variable more than once	Sergey Smolov	Sergey Smolov	1.0
9012	Retrascope Test Suite	Bug	Closed	Normal	VisBufferAllocVerilogPrinterTestCase: java.lang.IllegalArgumentException	Sergey Smolov		
9011	Retrascope Test Suite	Bug	Closed	Normal	Texas97IFetchVerilogPrinterTestCase: java.lang.IndexOutOfBoundsException: 4294967283 is out of bounds.	Sergey Smolov	Sergey Smolov	
9010	Retrascope Test Suite	Bug	Closed	Normal	Texas97CacheCoherenceVerilogPrinterTestCase: java.lang.IllegalArgumentException	Sergey Smolov	Sergey Smolov	
8994	Retrascope	Task	Closed	Normal	"BVEXTRACT(... BVEXTRACT (j i x))" expression transformation rule to the tool ruleset	Sergey Smolov	Sergey Smolov	1.0
8991	Retrascope	Bug	Closed	Normal	CfgSwitchSequenceBackend: do not collapse "if" statements with incompatible conditions	Sergey Smolov	Sergey Smolov	1.0
8990	Verilog Translator	Bug	Closed	High	vcegar-benchmarks/pi_bus/main_1.v: incorrect translation of nested "if" conditions	Sergey Smolov	Alexander Kamkin	0.1
8982	Verilog Translator	Task	New	Normal	"for" loop unrolling	Sergey Smolov	Alexander Kamkin	0.1

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8976	Retrascope	Task	Closed	Normal	Range: old -> high, young -> low	Sergey Smolov	Sergey Smolov	1.0
8975	Retrascope	Task	Closed	Normal	RetrascopeException.makeException -> RetrascopeException.exception	Sergey Smolov	Sergey Smolov	1.0
8957	Verilog Translator	Bug	Closed	High	wrong datatype for arrays	Sergey Smolov	Alexander Kamkin	0.1
8912	Retrascope	Bug	Closed	Normal	file ram.smv: line 332: variable is assigned more than once: m_ram.mem0	Sergey Smolov	Sergey Smolov	1.0
8874	Verilog Translator	Feature	Closed	High	mapping from instance variables to their code entries	Sergey Smolov	Alexander Kamkin	0.1
8871	QEMU4V	Feature	Closed	Normal	"-print-pte-addr" cmdline option	Sergey Smolov	Sergey Smolov	
8870	QEMU4V	Feature	Closed	Normal	trace generation for RISC-V programs	Sergey Smolov	Sergey Smolov	
8869	QEMU4V	Feature	Closed	Normal	trace generation for Aarch64 programs	Sergey Smolov	Sergey Smolov	
8868	QEMU4V	Feature	Closed	Normal	implement tracer that is activated by "-trace-log" command line option	Sergey Smolov	Sergey Smolov	
8867	QEMU4V	Feature	Closed	Normal	trace generation for PowerPC (32bit) programs	Sergey Smolov	Maxim Chudnov	0.3
8866	QEMU4V	Feature	Closed	Normal	trace generation for MIPS programs	Sergey Smolov	Maxim Chudnov	0.2
8865	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_19_11_00_1: java.lang.IllegalArgumentException: Declaration=DECLARATION(), parent=MODULE(m2)	Sergey Smolov	Alexander Kamkin	0.1
8864	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_17_10_02_1_i: java.lang.IllegalArgumentException	Sergey Smolov	Alexander Kamkin	0.1
8863	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_17_02_04_4_1: java.lang.IllegalArgumentException	Sergey Smolov	Alexander Kamkin	0.1
8862	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_12_08_02_1: java.lang.IllegalArgumentException	Sergey Smolov	Alexander Kamkin	0.1
8861	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_12_04_03_1: java.lang.IllegalStateException: BigInteger data is not convertible to Boolean.	Sergey Smolov	Alexander Kamkin	0.1
8860	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_12_04_02_4: java.lang.NullPointerException	Sergey Smolov	Alexander Kamkin	0.1
8859	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_12_04_02_3: java.lang.NullPointerException	Sergey Smolov	Alexander Kamkin	0.1
8858	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_12_04_01_2: java.lang.IllegalStateException: Parameter is not a value: (BVZEROEXT 2147483646 i)	Sergey Smolov	Alexander Kamkin	0.1
8857	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_12_02_02_2_1: java.lang.NullPointerException	Sergey Smolov	Alexander Kamkin	0.1
8856	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_10_04_05_1: java.lang.IllegalArgumentException	Sergey Smolov	Alexander Kamkin	0.1
8855	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_10_03_00_5: java.lang.IllegalArgumentException	Sergey Smolov	Alexander Kamkin	0.1
8854	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_05_02_02_2: java.lang.NullPointerException	Sergey Smolov	Alexander Kamkin	0.1

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8853	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_05_02_01_2: java.lang.IllegalArgumentException	Sergey Smolov	Alexander Kamkin	0.1
8852	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_05_01_14_4: java.lang.NullPointerException	Sergey Smolov	Alexander Kamkin	0.1
8851	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_05_01_14_3: java.lang.IllegalArgumentException: 0 must be > 0	Sergey Smolov	Alexander Kamkin	0.1
8850	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_05_01_14_1: java.lang.NullPointerException	Sergey Smolov	Alexander Kamkin	0.1
8849	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_04_10_01_1 [floating point parameters]: java.lang.IllegalArgumentException	Sergey Smolov	Alexander Kamkin	0.1
8848	Verilog Translator	Bug	Closed	Normal	test_07_08_00_1.v: Module 'pullup' cannot be found	Sergey Smolov	Alexander Kamkin	0.1
8847	Verilog Translator	Bug	Closed	Normal	test_17_01_01_2_1.v: Module 'pulldown' cannot be found	Sergey Smolov	Alexander Kamkin	0.1
8846	Verilog Translator	Bug	Closed	Normal	test_19_04_00_3.v: Module 'real_last' cannot be found	Sergey Smolov	Alexander Kamkin	0.1
8832	Verilog Translator	Bug	Closed	Normal	verilog/opencores/mips16/IF_stage.v: java.lang.IllegalStateException: Parameter is not a value: (BVSUB 8 1)	Sergey Smolov	Alexander Kamkin	0.1
8831	Verilog Translator	Bug	Closed	Normal	vcegar-benchmarks/ipbdp/ipbdp_hier.v: java.lang.IllegalArgumentException: Bit vector sizes do not match: 4 != 32.	Sergey Smolov	Alexander Kamkin	0.1
8786	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.sample.FifoTestbenchTestCase fails	Sergey Smolov	Sergey Smolov	0.1
8779	Verilog Translator	Bug	Closed	Normal	mips16/data_mem.v: wrong type for define-containing declaration of 'ram_addr' wire	Sergey Smolov	Alexander Kamkin	0.1
8738	Verilog Translator	Bug	Closed	Normal	DataMemTestCase falls with error	Sergey Smolov	Alexander Kamkin	0.1
8709	Fortress	Feature	Closed	Normal	'public static boolean isOperation(final Node node, final T ... opTypes)' convenience method	Sergey Smolov	Andrei Tatarnikov	0.4
8703	Fortress	Feature	Closed	Normal	'public static boolean isType(final Node node, final DataType ... types)' convenience method	Sergey Smolov	Andrei Tatarnikov	0.4
8702	Fortress	Feature	Closed	Normal	'public static NodeValue.newBitVector(final boolean value)' convenience method	Sergey Smolov	Andrei Tatarnikov	0.4
8681	Retrascope	Bug	Closed	Normal	EngineRegistry fails to create toolchain when HashSet\HashMap are used	Sergey Smolov	Alexander Kamkin	1.0
8667	Fortress	Feature	Closed	Normal	Nodes.EQ(Node ... nodes) convenience method	Sergey Smolov	Andrei Tatarnikov	0.4
8665	Fortress	Feature	Closed	High	Nodes.BVEXTRACT(Node, Node, Node) convenience method	Sergey Smolov	Andrei Tatarnikov	0.4
8615	Retrascope	Feature	Closed	Normal	"--no-backends" command line option	Sergey Smolov	Sergey Smolov	1.0
8587	MicroTESK	Feature	New	Normal	ISA subsets	Sergey Smolov	Artem Kotsynyak	2.6
8573	Fortress	Bug	Closed	Normal	missing javadoc	Sergey Smolov	Andrei Tatarnikov	0.4
8433	Trace Matcher	Feature	Closed	Normal	"--skip-equal" command line option	Sergey Smolov	Sergey Smolov	0.1

#	Project	Tracker	Status	Priority	Subject	Author	Assignee	Target version
8432	Trace Matcher	Task	Closed	Normal	register records: register names can contain all but space symbols	Sergey Smolov	Sergey Smolov	0.1
8430	Retrascope	Task	Closed	Normal	meta-info type for CFG statements that were added by HDL parser backends	Sergey Smolov	Sergey Smolov	1.0
8429	Retrascope	Task	Closed	Normal	backend that transforms "x[i] := y" assignments into constant-ranged	Sergey Smolov	Sergey Smolov	1.0
8305	Retrascope	Feature	Closed	Normal	EFSM state limit	Sergey Smolov	Sergey Smolov	0.2
8304	Retrascope	Feature	Rejected	Normal	SLR values number limit	Sergey Smolov	Sergey Smolov	0.2
8293	Retrascope	Task	Closed	Normal	add VeriTrans & Fortress info to NOTICE	Sergey Smolov	Sergey Smolov	0.2
8289	Retrascope	Bug	Closed	Normal	ITC99 b02: no resetting transition has been found	Sergey Smolov	Sergey Smolov	0.2
8288	Retrascope	Task	Closed	Normal	use DFS_NO_RPT walking where it is possible	Sergey Smolov	Sergey Smolov	0.2
8285	Retrascope	Bug	Closed	Normal	0% coverage of EFSM transitions for b01 example	Sergey Smolov	Sergey Smolov	0.2
8283	Retrascope	Bug	Closed	Normal	"X <= (others => '0')" should be translated properly when X is bit vector	Sergey Smolov	Sergey Smolov	0.2
8282	Retrascope	Feature	Closed	Normal	apply SLV detection heuristic to more than one CGAA path	Sergey Smolov	Sergey Smolov	0.2
8262	Retrascope	Feature	Closed	Normal	phase variable based approach for CFG-CGAA-EFSM optimisation	Sergey Smolov	Sergey Smolov	0.2
8260	Retrascope	Feature	Closed	Normal	VHDL record support (non-aggregate case)	Sergey Smolov	Maxim Chudnov	1.0
8245	Retrascope	Bug	Closed	Normal	cfg-rnd-testgen: IllegalArgumentException at minimips\pps_pf.v	Sergey Smolov	Sergey Smolov	0.2
8244	Retrascope	Bug	Closed	Normal	CGAA-to-EFSM engine falls on b05 test	Sergey Smolov	Sergey Smolov	0.2
8242	Trace Matcher	Bug	Closed	Normal	print hexadecimal values to the output file in the same form as they were at input flies	Sergey Smolov	Sergey Smolov	0.1
8237	Retrascope	Bug	Closed	Normal	CFG random test generator works too slow on b19	Sergey Smolov	Sergey Smolov	0.2
8220	Retrascope	Feature	Closed	Normal	BV_INC6 VHDL function support	Sergey Smolov	Sergey Smolov	0.2
8206	Trace Matcher	Feature	Closed	Normal	"--debug" command line option	Sergey Smolov	Sergey Smolov	0.1
8205	Verilog Translator	Task	Closed	Normal	Gradle-based build environment	Sergey Smolov	Sergey Smolov	0.1
8204	Fortress	Feature	Closed	Normal	solver-specific header for generated SMT2 files	Sergey Smolov	Sergey Smolov	0.4
8203	Fortress	Feature	Closed	Normal	bv2nat\int2bv operations	Sergey Smolov	Sergey Smolov	0.4
8199	Trace Matcher	Feature	Closed	Normal	"ignore-the-rest" command line option	Sergey Smolov	Sergey Smolov	0.1
8198	Trace Matcher	Feature	Closed	Normal	"exit-on-first-divergence" command line option	Sergey Smolov	Sergey Smolov	0.1
8197	Trace Matcher	Feature	Closed	Normal	"matching window in ticks" command line option	Sergey Smolov	Sergey Smolov	0.1
8194	Retrascope	Task	Closed	Normal	Separately solve independent sub-expressions of common AND expression	Sergey Smolov	Sergey Smolov	0.2
8184	Trace Matcher	Task	Closed	Normal	compare record fields in case insensitive mode	Sergey Smolov	Sergey Smolov	0.1
8181	Trace Matcher	Task	Closed	Normal	check whether trace records are ordered by time	Sergey Smolov	Sergey Smolov	0.1
8179	Trace Matcher	Task	Closed	Normal	ChangeLog	Sergey Smolov	Sergey Smolov	0.1
8167	QEMU4V	Task	New	Low	Program flow tracing	Sergey Smolov		
8161	Trace Matcher	Task	Closed	Normal	Basic modules	Sergey Smolov	Sergey Smolov	0.1
8113	Trace Matcher	Task	Closed	Normal	Gradle build environment	Sergey Smolov	Sergey Smolov	0.1

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7972	Retrascope	Task	Closed	Normal	empty event-free cases merging backend	Sergey Smolov	Sergey Smolov	0.2
7906	Retrascope	Task	Closed	Normal	Backend that merges "neighbour ranged" sequential 'if' statements	Sergey Smolov	Sergey Smolov	0.2
7883	Retrascope	Bug	Closed	Normal	fifo_testbench.v: java.lang.NullPointerException	Sergey Smolov	Sergey Smolov	0.2
7846	Fortress	Task	Rejected	Normal	'Transformer.reduce(Transformer.substitute(expression, name, term))' convenience method	Sergey Smolov		0.4
7806	Retrascope	Task	Closed	Normal	[cgaa] process - collection of diagrams	Sergey Smolov	Sergey Smolov	0.2
7772	Fortress	Task	Closed	High	TypeConversion.coerce: transform from MAP to BIT_VECTOR	Sergey Smolov	Sergey Smolov	0.4
7770	Retrascope	Task	Closed	Normal	'others' attribute upon array/bitvector initialization	Sergey Smolov	Sergey Smolov	1.0
7753	Retrascope	Bug	Closed	Normal	example.vhd: cannot generate SMV-based test	Sergey Smolov	Sergey Smolov	0.2
7742	Retrascope	Task	Closed	Normal	enum support	Sergey Smolov	Sergey Smolov	0.2
7733	Trace Matcher	Task	Closed	Normal	run.bat script for Windows	Sergey Smolov	Sergey Smolov	0.1
7732	Trace Matcher	Task	Closed	Normal	oracle: record queue based comparison approach	Sergey Smolov	Sergey Smolov	0.1
7730	MicroTESK	Bug	Closed	High	[tarmac-logger] missing "<cpu>" tag	Sergey Smolov	Andrei Tatarnikov	2.4
7727	Retrascope	Task	Closed	Normal	Flatten module instances	Sergey Smolov	Sergey Smolov	0.2
7725	Verilog Translator	Task	Closed	Normal	bitvector arrays support	Sergey Smolov	Alexander Kamkin	0.1
7723	Retrascope	Task	Rejected	Normal	Support for module instances in Verilog descriptions	Sergey Smolov	Sergey Smolov	1.0
7720	Retrascope	Bug	Closed	Normal	mips16/data_mem.v: The expression to be computed (ram) contains unevaluated variables: [ram]	Sergey Smolov	Sergey Smolov	0.2
7715	Retrascope	Task	Closed	Normal	[refactoring] duplicate code in AssertionVariableContainer	Sergey Smolov	Sergey Smolov	0.2
7663	Trace Matcher	Task	Closed	Normal	"main" function	Sergey Smolov	Sergey Smolov	0.1
7626	Retrascope	Task	Closed	Normal	HDL Retrascope 0.2.2-beta release	Sergey Smolov	Sergey Smolov	0.2
7623	Retrascope	Task	Closed	Normal	HLDD-to-SMV printer with no assertions	Sergey Smolov	Sergey Smolov	0.2
7597	Retrascope	Task	Closed	Normal	EfsmTransition.getGuardedAction().getGuard() -> EfsmTransition.getGuard()	Sergey Smolov	Sergey Smolov	0.2
7595	Retrascope	Task	Closed	Normal	GuardedAction.getGuard().getNode() -> GuardedAction.getGuardNode()	Sergey Smolov	Sergey Smolov	0.2
7594	Retrascope	Bug	Rejected	Normal	ModelSim shows error when TST file contains multiple comments	Sergey Smolov	Sergey Smolov	0.2
7593	Retrascope	Bug	Closed	Normal	mips16\data_mem.v: java.lang.IllegalArgumentException	Sergey Smolov	Sergey Smolov	0.2
7576	Retrascope	Bug	Closed	Normal	mips16/hazard_detection_unit.v: java.lang.IllegalArgumentException: Constraint contains errors	Sergey Smolov	Sergey Smolov	0.2
7574	Retrascope	Task	Closed	Normal	Efsm: deepCopy()	Sergey Smolov	Sergey Smolov	0.2
7564	MicroTESK	Task	Closed	Normal	"How to build MicroTESK" guide for developers in project Wiki	Sergey Smolov	Alexander Kamkin	2.5
7561	Fortress	Task	New	Normal	ISampleConstraint: 'getExpectedVariables' returns value that is ignored in jUnit tests	Sergey Smolov	Andrei Tatarnikov	0.4
7557	Fortress	Bug	Closed	High	ConstCastTestCase: java.lang.AssertionError: Calculator failed to substitute result	Sergey Smolov	Artem Kotsynyak	0.4
7555	Fortress	Bug	Closed	Normal	unable to create constraint-related jUnit tests including unused variables	Sergey Smolov	Artem Kotsynyak	0.4

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7546	Retrascope	Task	Closed	Normal	Print tool execution time in milliseconds	Sergey Smolov	Sergey Smolov	0.2
7527	Fortress	Task	Closed	Normal	constant casting while type conversion	Sergey Smolov	Sergey Smolov	0.4
7524	Verilog Translator	Task	Closed	Normal	support for non-zero-starting bit vector variables & signals	Sergey Smolov	Sergey Smolov	0.1
7474	Verilog Translator	Bug	Closed	Normal	missing empty branches for 'if' statements	Sergey Smolov	Sergey Smolov	0.1
7423	Retrascope	Bug	Rejected	High	rnd_fsm.vhd: empty tst file	Sergey Smolov	Igor Melnichenko	0.2
7409	Retrascope	Task	Closed	Normal	EFSM state abstraction (stabilization)	Sergey Smolov	Sergey Smolov	0.2
7402	Fortress	Task	Closed	Normal	ExprUtils: ignore repeated Node objects upon conjunction/disjunction construction	Sergey Smolov	Andrei Tatarnikov	0.4
7397	Fortress	Task	Closed	Normal	NodeVariable.new<type-of-variable>(final String name)	Sergey Smolov	Andrei Tatarnikov	0.4
7383	Fortress	Task	Closed	Normal	boolean isOperation(final Node expr, final T... opId)	Sergey Smolov	Andrei Tatarnikov	0.4
7378	Fortress	Task	Closed	Low	NodeTransformer: multiple transform rules for a single enum id	Sergey Smolov	Artem Kotsynyak	0.4
7271	Retrascope	Task	Closed	Normal	add javadoc for new methods when efsm.state.abstraction branch will be merged into master	Sergey Smolov	Sergey Smolov	0.2
7166	Retrascope	Bug	Closed	Normal	cfg-rnd-testgen: OutOfMemoryError at b10 (1.000.000 ticks)	Sergey Smolov	Sergey Smolov	0.2
7145	Retrascope	Bug	Closed	Normal	cfg-rnd-testgen: take variable invariants into account	Sergey Smolov	Sergey Smolov	0.2
7104	Retrascope	Task	Closed	High	smv-test-parser: filter tests	Sergey Smolov	Sergey Smolov	0.2
7098	Verilog Translator	Bug	Closed	Normal	src/test/verilog/mips16/data_mem.v: 'mem_access_addr' has null declaration	Sergey Smolov	Sergey Smolov	0.1
7097	Retrascope	Bug	Closed	Normal	32-bit constants should be casted to appropriate values	Sergey Smolov	Sergey Smolov	0.2
7096	Retrascope	Task	Closed	Normal	assign process merging backend	Sergey Smolov	Sergey Smolov	0.2
7081	Retrascope	Task	Rejected	Normal	xor-composition-printer	Sergey Smolov	Sergey Smolov	0.2
6990	Retrascope IDE	Task	Rejected	Normal	use veditor 1.2.1c	Sergey Smolov	Sergey Smolov	0.1
6989	Retrascope IDE	Task	Rejected	Normal	migrate to Eclipse Mars (4.5)	Sergey Smolov	Sergey Smolov	0.1
6988	Retrascope IDE	Task	New	Normal	[efsm][visualizator][zest] "organic" layout for EFSM models	Sergey Smolov		0.1
6984	Retrascope IDE	Bug	Closed	Normal	java.io.IOException: Unable to resolve plug-in "platform:/plugin/retrascope-ide/icons/retrascope.gif".	Sergey Smolov	Sergey Smolov	0.1
6983	Retrascope IDE	Task	Closed	Normal	[cfg][visualizator][zest] visualize CfgAssertStatement & CfgLoopStatement nodes	Sergey Smolov	Sergey Smolov	0.1
6976	Retrascope	Task	Closed	Normal	Wiki update	Sergey Smolov	Sergey Smolov	0.2
6959	Retrascope IDE	Bug	Closed	High	java.lang.NullPointerException at startup	Sergey Smolov	Sergey Smolov	0.1
6956	Retrascope	Task	Closed	Normal	HDL Retrascope 0.2.1 release	Sergey Smolov	Sergey Smolov	0.2
6892	Retrascope	Bug	Closed	Normal	support for non-zero starting bitvectors	Sergey Smolov	Sergey Smolov	0.2
6864	Retrascope	Task	Closed	Normal	Remove crypto-cores from test suite	Sergey Smolov	Igor Melnichenko	0.1
6831	Fortress	Task	Closed	Normal	ESExprParser: improve error messages	Sergey Smolov	Artem Kotsynyak	0.4
6808	Retrascope	Task	Rejected	High	Split CFG processes into independent parts	Sergey Smolov	Sergey Smolov	0.2

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6758	Retrascope	Task	Closed	Normal	return state/transition coverage for the specified EFSM & test entities	Sergey Smolov	Sergey Smolov	0.2
6730	Retrascope	Bug	Closed	Normal	fix javadoc	Sergey Smolov	Mikhail Lebedev	0.1
6537	Retrascope	Developer Request	Closed	Normal	Efsm: collection of resetting guarded actions	Sergey Smolov	Igor Melnichenko	0.1
6534	Retrascope	Task	Closed	Normal	pass reset-like signals to EFSM-based assertions	Sergey Smolov	Sergey Smolov	0.1
6528	Retrascope	Task	Closed	Normal	random test generator	Sergey Smolov	Sergey Smolov	0.1
6511	Retrascope	Task	Rejected	Normal	keep expressions at case statements	Sergey Smolov	Sergey Smolov	0.1
6510	Retrascope	Bug	Closed	Normal	fix javadoc	Sergey Smolov	Mikhail Lebedev	0.1
6509	Retrascope	Task	Rejected	Normal	merge embedded switch nodes with conditions depending exactly from the same variable(s)	Sergey Smolov	Sergey Smolov	0.1
6507	Castle	Task	Closed	Normal	build.gradle: get ANTLR jar from server	Sergey Smolov	Sergey Smolov	
6504	Retrascope	Bug	Closed	Normal	fifo/fifo.v: nuSMV model checker returns ERROR	Sergey Smolov	Mikhail Lebedev	0.1
6490	Retrascope	Task	Closed	High	Gradle task & cmdline scripts for running the tool from terminal	Sergey Smolov	Sergey Smolov	0.1
6483	Retrascope	Task	Closed	High	keep related clock-like variables for top-level containers of EFSM assertions	Sergey Smolov	Sergey Smolov	0.1
6472	Retrascope	Task	Closed	Normal	b13.vhd: too long elaboration time	Sergey Smolov	Mikhail Lebedev	1.0
6456	Retrascope	Task	Closed	High	CFG model as hirerarchical list of statements	Sergey Smolov	Sergey Smolov	0.1
6454	Retrascope	Task	Closed	Normal	group sequential switches with boolean conditions of "x == a" form	Sergey Smolov	Sergey Smolov	0.1
6453	Retrascope	Task	Closed	Normal	Statement class for grouping CFG nodes	Sergey Smolov	Sergey Smolov	0.1
6449	Retrascope	Task	New	Low	testbench generator taking test sequences and mappings as inputs	Sergey Smolov	Sergey Smolov	2.0
6448	Retrascope	Task	New	Low	mapping description language + IR + parser	Sergey Smolov	Sergey Smolov	2.0
6447	Retrascope	Task	Closed	Normal	SMV-based counterexamples parser	Sergey Smolov	Mikhail Lebedev	0.2
6446	Retrascope	Task	New	Normal	Promela translator to CFG representation (no buffers)	Sergey Smolov	Mikhail Lebedev	2.0
6445	Retrascope	Task	Closed	Normal	compare nuXmv and NuSMV	Sergey Smolov	Mikhail Lebedev	0.1
6443	Retrascope	Bug	Closed	Normal	print error message when "--toplevel" value is wrong	Sergey Smolov	Sergey Smolov	0.1
6431	Retrascope	Task	Closed	Normal	descriptor for (VHDL) variables & signals	Sergey Smolov	Sergey Smolov	0.1
6430	Retrascope	Bug	Closed	Normal	b14.vhd: StackOverflowError	Sergey Smolov	Sergey Smolov	0.2
6426	Retrascope	Bug	Closed	Normal	example.vhd: HlddXmvVisitor.onProcessEnd(HlddXmvVisitor.java:381) -> NullPointerException	Sergey Smolov	Mikhail Lebedev	0.1
6425	Retrascope	Bug	Closed	Normal	b12.vhd: XmvExprPrinter.getConstant(XmvExprPrinter.java:330) -> NullPointerException	Sergey Smolov	Mikhail Lebedev	0.1
6424	Retrascope	Bug	Closed	Normal	b05.vhd: line 64: at token "d32_-10": syntax error	Sergey Smolov	Mikhail Lebedev	0.1
6423	Fortress	Task	Rejected	Low	to_real, to_int, is_int operations	Sergey Smolov	Andrei Tatarnikov	0.4
6413	Retrascope	Bug	Closed	Normal	b03.vhd: different EFSM extraction stats	Sergey Smolov	Sergey Smolov	0.1
6412	Retrascope	Task	Rejected	Normal	engine combining HLDD & assertion model	Sergey Smolov	Sergey Smolov	0.1
6410	Retrascope	Task	Closed	Normal	no-loop/no-recursion functions elaboration	Sergey Smolov	Sergey Smolov	0.1

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6394	Local Support Project	Bug	New	Normal	Проект HDL Retrascope: на 17-дюймовом мониторе не масштабируется таблица Задачи	Sergey Smolov	Alexey Demakov	
6393	Retrascope	Task	Rejected	Normal	migrate to EFSM model containing only concurrent assignments	Sergey Smolov	Igor Melnichenko	0.2
6389	Retrascope	Task	Closed	Normal	Wiki documentation about testbench simulation	Sergey Smolov	Sergey Smolov	0.1
6375	Retrascope	Bug	Closed	Normal	missing javadoc	Sergey Smolov	Igor Melnichenko	0.1
6367	Retrascope	Task	Closed	Urgent	Fortress expressions printing in an SMV format	Sergey Smolov	Mikhail Lebedev	0.1
6366	Retrascope	Bug	Rejected	Normal	src/test/vhdl/example/test.vhd: Efsm.UNINITIALISED_STATE isn't supported yet	Sergey Smolov	Igor Melnichenko	0.2
6365	Retrascope	Bug	Closed	Normal	src/test/vhdl/example/example.vhd: IllegalArgumentException	Sergey Smolov	Mikhail Lebedev	0.1
6364	Fortress	Task	Rejected	Low	SolverResult: implement equals\hashcode methods	Sergey Smolov	Andrei Tatarnikov	0.4
6363	Verilog Translator	Bug	Closed	High	src/test/verilog/fifo0/mem_2p.v: AbstractMethodError	Sergey Smolov	Alexander Kamkin	0.1
6362	Retrascope	Bug	Rejected	Normal	src/test/verilog/adder/adder4_testbench.v: wrong CFG model	Sergey Smolov	Mikhail Chupilko	0.1
6355	Verilog Translator	Bug	Closed	High	src/test/verilog/fifo/fifo_testbench.v: NullPointerException	Sergey Smolov	Alexander Kamkin	0.1
6354	Retrascope	Task	Closed	Normal	Collapsing group node for Module	Sergey Smolov	Alexander Protsenko	0.1
6353	Retrascope	Bug	Closed	Normal	Case children of one Switch node can have equal NodeValue	Sergey Smolov	Sergey Smolov	0.1
6352	Fortress	Bug	Closed	High	Transformer.standardize returns 'false' on (AND (EQ a 00) (NOT(EQ a b 00)))	Sergey Smolov	Artem Kotsynyak	0.4
6350	Retrascope	Task	Closed	Normal	EfsmConflictExtractor wiki documentation	Sergey Smolov	Mikhail Lebedev	0.1
6336	Retrascope	Task	Closed	Normal	jUnit tests for EfsmConflictExtractor	Sergey Smolov	Mikhail Lebedev	0.1
6335	Retrascope	Bug	Closed	Normal	fifo.v: non-constant number of extracted EFSMs' transitions	Sergey Smolov	Sergey Smolov	0.1
6331	Retrascope	Task	Closed	Normal	look into unused classes	Sergey Smolov	Sergey Smolov	
6327	Retrascope	Task	Closed	Normal	log messages class	Sergey Smolov	Sergey Smolov	0.1
6301	Retrascope	Task	Closed	Normal	unused code	Sergey Smolov	Sergey Smolov	1.0
6293	Retrascope	Bug	Closed	Normal	XmlTestParserTestCase: NoSuchMethodException	Sergey Smolov	Igor Melnichenko	0.1
6282	Retrascope	Task	Closed	High	finish AstSmvVisitor & CfgAstVisitor merge	Sergey Smolov	Mikhail Lebedev	0.1
6281	Retrascope	Bug	Closed	Normal	EfsmTestGeneratorVhdlTestCase: Efsm.UNINITIALISED_STATE isn't supported yet	Sergey Smolov	Sergey Smolov	0.1
6280	Retrascope	Bug	Closed	Normal	TestVhdlTestbenchPrinterVhdlTestCase: The exception has occurred while printing test pattern file	Sergey Smolov	Igor Melnichenko	0.1
6279	Retrascope	Bug	Closed	Normal	TestXmlPrinterTestCase: IllegalArgumentException: Output file name isn't specified	Sergey Smolov	Igor Melnichenko	0.1
6263	Retrascope	Bug	Closed	High	Crash when test generation engine elaborates EFSMs from alu.vhd: java.lang.IllegalArgumentException	Sergey Smolov	Sergey Smolov	0.2
6241	MicroTESK	Bug	Closed	Normal	Generated assembler files contain tab-only lines	Sergey Smolov	Andrei Tatarnikov	2.2
6108	MicroTESK	Task	Closed	Normal	create environment variable(s) for SMT solver(s)	Sergey Smolov	Andrei Tatarnikov	2.2

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6106	MicroTESK	Bug	Closed	Normal	zero opcodes for instructions in Tarmac log	Sergey Smolov	Andrei Tatarnikov	2.2
6061	Retrascope	Task	Closed	Normal	EFSM-based transition assertion generator	Sergey Smolov	Sergey Smolov	1.0
6060	Retrascope	Task	Closed	Normal	Add plasma to project test suite	Sergey Smolov	Sergey Smolov	0.2
6059	Retrascope	Task	Closed	Normal	Simple solver for "x && !x" constraints	Sergey Smolov	Sergey Smolov	0.1
6051	Retrascope	Task	Closed	Normal	state-like variable names option	Sergey Smolov	Sergey Smolov	0.1
6050	Retrascope	Task	Closed	High	Path to testbench directory as command-line parameter	Sergey Smolov	Igor Melnichenko	0.1
6049	Retrascope	Task	Closed	Normal	VHDL test printer: write documentation to project wiki	Sergey Smolov	Igor Melnichenko	0.1
6041	Retrascope	Task	Closed	Normal	move to gradle based build system	Sergey Smolov	Sergey Smolov	0.1
5993	Fortress	Task	Closed	Normal	boolean ExprUtils.isKind(Node.Kind kind, Node ... nodes)	Sergey Smolov	Andrei Tatarnikov	0.4
5985	Fortress	Task	Closed	High	Node ExprUtils.getEquation(Node target, Node value)	Sergey Smolov	Andrei Tatarnikov	0.4
5967	MicroTESK	Task	Closed	Low	one directory for all components of distribution	Sergey Smolov	Andrei Tatarnikov	2.2
5966	MicroTESK	Bug	Closed	Normal	mark shell scripts as executable in the distribution tar.gz archive	Sergey Smolov	Sergey Smolov	2.5
5907	Fortress	Task	Closed	Normal	boolean areOfType(DataTypeId id, Node ... nodes)	Sergey Smolov	Andrei Tatarnikov	0.3
5904	Retrascope	Task	Closed	Normal	save jUnit test results in build/test-results	Sergey Smolov	Sergey Smolov	0.1
5897	Retrascope	Task	Closed	Normal	fix javadoc for methods using InvariantChecks.checkNotNull	Sergey Smolov	Sergey Smolov	0.1
5896	Retrascope	Task	Closed	Normal	remove parameterized collections from public method interfaces	Sergey Smolov	Sergey Smolov	0.1
5887	Retrascope	Task	Closed	Normal	rename 'decider_parser.vhd'	Sergey Smolov	Igor Melnichenko	0.1
5881	Verilog Translator	Task	Closed	Normal	keep file names in the AST top nodes	Sergey Smolov	Sergey Smolov	0.1
5875	Retrascope	Task	Closed	Normal	Check state/transition count for extracted EFSM models	Sergey Smolov	Sergey Smolov	0.1
5873	Retrascope	Bug	Closed	High	missing transitions in b04 EFSM	Sergey Smolov	Sergey Smolov	0.1
5872	Retrascope	Task	Closed	Normal	HDL file meta info	Sergey Smolov	Sergey Smolov	0.1
5871	Retrascope	Bug	Closed	Normal	ru.ispras.retrascope.test.printer.testbench -> ru.ispras.retrascope.engine.test.printer.testbench	Sergey Smolov	Igor Melnichenko	0.1
5870	Retrascope	Task	Closed	Normal	Retrascope exceptions	Sergey Smolov	Igor Melnichenko	0.1
5868	Retrascope	Task	Closed	Normal	Migrate to Fortress 0.4	Sergey Smolov	Sergey Smolov	0.1
5861	Fortress	Task	Closed	Low	static boolean containsSingleObject(Collection<?> collection)	Sergey Smolov	Andrei Tatarnikov	0.3
5836	Local Support Project	Bug	Resolved	High	не собирается проект на сервере Jenkins	Sergey Smolov	Sergey Smolov	
5832	Retrascope	Task	Closed	Normal	print some info about failed tests	Sergey Smolov	Sergey Smolov	0.1
5831	Retrascope	Bug	Closed	Normal	EfsmSimulator.java -> Tag @see: can't find getResetGuardedAction() in ru.ispras.retrascope.model.efsm.Efsm	Sergey Smolov	Igor Melnichenko	0.1
5828	Retrascope	Bug	Closed	Normal	TestVhdlTestbenchPrinterVhdlTestCase -> IllegalArgumentException: Unexpected event value: true	Sergey Smolov	Igor Melnichenko	0.1

#	Project	Tracker	Status	Priority	Subject	Author	Assignee	Target version
5827	Retrascope	Bug	Closed	Normal	TestVhdlTestbenchPrinterDummyTestCase -> NoSuchFileException	Sergey Smolov	Igor Melnichenko	0.1
5802	Fortress	Task	Closed	High	NodeValue newZero(DataType dataType)	Sergey Smolov	Andrei Tatarnikov	0.3
5778	Retrascope	Bug	Closed	Normal	ru.ispras.retrascope.engine.testbench.TestVhdlTestbenchPrinterTestCase -> java.util.NoSuchElementException	Sergey Smolov	Igor Melnichenko	0.1
5756	Retrascope	Task	Closed	Normal	EFSM pre-initial state + initialization action	Sergey Smolov	Sergey Smolov	0.1
5755	Retrascope	Task	Closed	Low	use Zamia IG visitors & walkers	Sergey Smolov	Sergey Smolov	0.1
5736	Retrascope	Bug	Closed	Normal	EfsmSimulator.substituteVariables(EfsmSimulator.java:736) -> NullPointerException	Sergey Smolov	Igor Melnichenko	0.1
5719	Retrascope	Bug	Closed	Urgent	EFSM Test Generator hangs on b11	Sergey Smolov	Igor Melnichenko	0.1
5715	Retrascope	Bug	Closed	High	EfsmTestGenerator.java:138: error: method put in interface Map<K,V> cannot be applied to given types -> traversedPaths.put(efsm, new HashSet<>());	Sergey Smolov	Igor Melnichenko	0.1
5711	Retrascope	Task	Closed	Normal	Check generated *.smv files with external model checker	Sergey Smolov	Mikhail Lebedev	1.0
5709	Retrascope	Bug	Closed	Normal	TestMinimiser.java:43: warning - @param argument "test" is not a parameter name.	Sergey Smolov	Igor Melnichenko	0.1
5704	Retrascope	Task	Closed	Normal	try to find a way to remove 'toplevel' option	Sergey Smolov	Sergey Smolov	0.1
5702	Retrascope IDE	Task	New	Normal	[tool] create Retrascope icon	Sergey Smolov		0.1
5696	Retrascope	Task	Closed	Normal	exclude sandbox & test folder from distribution	Sergey Smolov	Sergey Smolov	0.1
5695	Retrascope	Task	Closed	Normal	mark retrascope.sh as executable automatically	Sergey Smolov	Sergey Smolov	0.1
5694	Retrascope	Task	Closed	Normal	collect the *.smt2 files and analyse constraints	Sergey Smolov	Sergey Smolov	0.1
5692	Retrascope	Bug	Rejected	Normal	FATE/FATE+ hangs on b03 with Java 1.8	Sergey Smolov	Igor Melnichenko	
5689	Retrascope	Task	Closed	High	implement test-to-Verilog printer	Sergey Smolov	Sergey Smolov	0.2
5688	Retrascope	Task	Closed	Normal	implement test-to-VHDL printer	Sergey Smolov	Igor Melnichenko	0.1
5684	Retrascope	Bug	Rejected	Low	computeExpression -> LOGIC_BOOLEAN vs (MAP LOGIC_INTEGER LOGIC_BOOLEAN)	Sergey Smolov	Igor Melnichenko	0.2
5683	Retrascope	Task	Closed	Normal	STD_LOGIC/STD_ULOGIC processing	Sergey Smolov	Sergey Smolov	0.1

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