## Issues

| # | Project | Tracker | Status | Priority | Subject | Author | Assignee | Target version |
|---|---|---|---|---|---|---|---|---|
| 6108 | MicroTESK | Task | Closed | Normal | create environment variable(s) for SMT solver(s) | Sergey Smolov | Andrei Tatarnikov | 2.2 |
| 5967 | MicroTESK | Task | Closed | Low | one directory for all components of distribution | Sergey Smolov | Andrei Tatarnikov | 2.2 |
| 4674 | TestBase | Task | New | Normal | Тестовые ситуации | Sergey Smolov | Artem Kotsynyak | 0.0 |
| 3914 | Fortress | Task | Rejected | Normal | function templates | Sergey Smolov | Andrei Tatarnikov | 0.1 |
| 4175 | Fortress | Task | Closed | Normal | Добавить параметризованные операции | Sergey Smolov | Sergey Smolov | 0.1 |
| 4133 | Fortress | Task | Closed | Normal | ABS, MAX, MIN для Logic-типов | Sergey Smolov | Sergey Smolov | 0.1 |
| 3973 | Fortress | Task | Closed | Normal | Реализовать добавление Variable в Constraint | Sergey Smolov | Sergey Smolov | 0.1 |
| 9904 | Verilog Translator | Task | Closed | Normal | add info for "--library-file" cmdline option | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9859 | Verilog Translator | Task | New | Normal | modify "ERROR: [Internal] null" line at error log | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9790 | Verilog Translator | Task | New | Normal | external names for unnamed generate blocks | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9251 | Verilog Translator | Task | Closed | High | calculate type of index for bit-vector arrays | Sergey Smolov | Alexander Kamkin | 0.1 |
| 8982 | Verilog Translator | Task | New | Normal | "for" loop unrolling | Sergey Smolov | Alexander Kamkin | 0.1 |
| 7725 | Verilog Translator | Task | Closed | Normal | bitvector arrays support | Sergey Smolov | Alexander Kamkin | 0.1 |
| 5455 | Verilog Translator | Task | Closed | Normal | устранить зависимость от ANTLRWorks | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9899 | Verilog Translator | Task | Closed | Normal | VerilogPrinter test cases for QUIP benchmarks | Sergey Smolov | Maxim Chudnov | 0.1 |
| 9232 | Verilog Translator | Task | Closed | High | remove typedefs from texas97-tests/PPC60X_bus/src/define.v | Sergey Smolov | Mikhail Lebedev | 0.1 |
| 10009 | Verilog Translator | Task | Closed | Normal | README\ChangeLog -> README.md\ChangeLog.md | Sergey Smolov | Sergey Smolov | 0.1 |
| 9771 | Verilog Translator | Task | Closed | Normal | fix 'publishing' block behaviour for Gradle 4.10.3 | Sergey Smolov | Sergey Smolov | 0.1 |
| 9311 | Verilog Translator | Task | Closed | High | type casting of expression operands | Sergey Smolov | Sergey Smolov | 0.1 |
| 9208 | Verilog Translator | Task | Closed | Normal | add Verilog2Smv\VIS benchmark to project test suite | Sergey Smolov | Sergey Smolov | 0.1 |
| 9207 | Verilog Translator | Task | Closed | Normal | add VCEGAR benchmark to project test suite | Sergey Smolov | Sergey Smolov | 0.1 |

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| 9206 | Verilog Translator | Task | Closed | Normal | add Texas97 benchmark to project test suite | Sergey Smolov | Sergey Smolov | 0.1 |
| 8205 | Verilog Translator | Task | Closed | Normal | Gradle-based build environment | Sergey Smolov | Sergey Smolov | 0.1 |
| 7524 | Verilog Translator | Task | Closed | Normal | support for non-zero-starting bit vector variables & signals | Sergey Smolov | Sergey Smolov | 0.1 |
| 5881 | Verilog Translator | Task | Closed | Normal | keep file names in the AST top nodes | Sergey Smolov | Sergey Smolov | 0.1 |
| 5651 | Verilog Translator | Task | Closed | Normal | Translate logic operation results into Boolean expressions | Sergey Smolov | Sergey Smolov | 0.1 |
| 5258 | Retrascope | Task | Closed | High | [basis] Обработка циклических зависимостей разных Engine | Sergey Smolov | Alexander Kamkin | 0.1 |
| 5249 | Retrascope | Task | Closed | High | [basis] Настройка Retrascope для работы с SMT-решателями | Sergey Smolov | Alexander Kamkin | 0.1 |
| 5247 | Retrascope | Task | Closed | Normal | [basis] Набор идентификаторов Engine как опция командной строки Retrascope | Sergey Smolov | Alexander Kamkin | 0.1 |
| 4946 | Retrascope | Task | Closed | Normal | [basis][log] Ведение лога для нескольких логгеров | Sergey Smolov | Alexander Kamkin | 0.1 |
| 4945 | Retrascope | Task | Closed | Normal | [basis][log] Опция логирования | Sergey Smolov | Alexander Kamkin | 0.1 |
| 6354 | Retrascope | Task | Closed | Normal | Collapsing group node for Module | Sergey Smolov | Alexander Protsenko | 0.1 |
| 6864 | Retrascope | Task | Closed | Normal | Remove crypto-cores from test suite | Sergey Smolov | Igor Melnichenko | 0.1 |
| 6050 | Retrascope | Task | Closed | High | Path to testbench directory as command-line parameter | Sergey Smolov | Igor Melnichenko | 0.1 |
| 6049 | Retrascope | Task | Closed | Normal | VHDL test printer: write documentation to project wiki | Sergey Smolov | Igor Melnichenko | 0.1 |
| 5887 | Retrascope | Task | Closed | Normal | rename 'decider_parser.vhd' | Sergey Smolov | Igor Melnichenko | 0.1 |
| 5870 | Retrascope | Task | Closed | Normal | Retrascope exceptions | Sergey Smolov | Igor Melnichenko | 0.1 |
| 5688 | Retrascope | Task | Closed | Normal | implement test-to-VHDL printer | Sergey Smolov | Igor Melnichenko | 0.1 |
| 5537 | Retrascope | Task | Closed | Normal | [efsm][generator][test] make log shorter | Sergey Smolov | Igor Melnichenko | 0.1 |
| 5501 | Retrascope | Task | Closed | Normal | [efsm][generator][test] Class 'EfsmAtomicTestGenerator' is never used | Sergey Smolov | Igor Melnichenko | 0.1 |
| 5498 | Retrascope | Task | Closed | Normal | [model][basis][memory] rename IMemory interface | Sergey Smolov | Igor Melnichenko | 0.1 |
| 5495 | Retrascope | Task | Closed | Normal | [structure] move ru.ispras.retrascope.testbench.media package to ru.ispras.retrascope.result.testbench | Sergey Smolov | Igor Melnichenko | 0.1 |
| 5494 | Retrascope | Task | Closed | Normal | [structure] remove ru.ispras.retrascope.engine.efsm.testgen.heuristic empty package | Sergey Smolov | Igor Melnichenko | 0.1 |
| 5471 | Retrascope | Task | Closed | Normal | [structure] Rename *ing packages | Sergey Smolov | Igor Melnichenko | 0.1 |
| 5456 | Retrascope | Task | Closed | Normal | [structure] Замечания по структуре каталогов | Sergey Smolov | Igor Melnichenko | 0.1 |
| 5420 | Retrascope | Task | Closed | Normal | [util] метод fillNodeWithValues заменить на Transformer.substituteAllBindings | Sergey Smolov | Igor Melnichenko | 0.1 |
| 4359 | Retrascope | Task | Rejected | Normal | [cfg] Реализовать метод toConstraint() | Sergey Smolov | Igor Melnichenko | 0.1 |
| 5578 | Retrascope | Task | Closed | Normal | [verilog][parser][cfg] add support of multiple assignments | Sergey Smolov | Mikhail Chupilko | 0.1 |
| 5398 | Retrascope | Task | Closed | Normal | [verilog][parser][cfg] Преобразование констант в NodeValue | Sergey Smolov | Mikhail Chupilko | 0.1 |

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|---|---|---|---|---|---|---|---|---|
| 6445 | Retrascope | Task | Closed | Normal | compare nuXmv and NuSMV | Sergey Smolov | Mikhail Lebedev | 0.1 |
| 6367 | Retrascope | Task | Closed | Urgent | Fortress expressions printing in an SMV format | Sergey Smolov | Mikhail Lebedev | 0.1 |
| 6350 | Retrascope | Task | Closed | Normal | EfsmConflictExtractor wiki documentation | Sergey Smolov | Mikhail Lebedev | 0.1 |
| 6336 | Retrascope | Task | Closed | Normal | jUnit tests for EfsmConflictExtractor | Sergey Smolov | Mikhail Lebedev | 0.1 |
| 6282 | Retrascope | Task | Closed | High | finish AstSmvVisitor & CfgAstVisitor merge | Sergey Smolov | Mikhail Lebedev | 0.1 |
| 5541 | Retrascope | Task | Closed | High | [engine][printer][smv] move engine.printer.smv package to sandbox | Sergey Smolov | Mikhail Lebedev | 0.1 |
| 5497 | Retrascope | Task | Closed | Normal | [efsm][extractor][conflict][jaxb] rename jaxb-classes | Sergey Smolov | Mikhail Lebedev | 0.1 |
| 6534 | Retrascope | Task | Closed | Normal | pass reset-like signals to EFSM-based assertions | Sergey Smolov | Sergey Smolov | 0.1 |
| 6528 | Retrascope | Task | Closed | Normal | random test generator | Sergey Smolov | Sergey Smolov | 0.1 |
| 6511 | Retrascope | Task | Rejected | Normal | keep expressions at case statements | Sergey Smolov | Sergey Smolov | 0.1 |
| 6509 | Retrascope | Task | Rejected | Normal | merge embedded switch nodes with conditions depending exactly from the same variable(s) | Sergey Smolov | Sergey Smolov | 0.1 |
| 6490 | Retrascope | Task | Closed | High | Gradle task & cmdline scripts for running the tool from terminal | Sergey Smolov | Sergey Smolov | 0.1 |
| 6483 | Retrascope | Task | Closed | High | keep related clock-like variables for top-level containers of EFSM assertions | Sergey Smolov | Sergey Smolov | 0.1 |
| 6456 | Retrascope | Task | Closed | High | CFG model as hirerarchical list of statements | Sergey Smolov | Sergey Smolov | 0.1 |
| 6454 | Retrascope | Task | Closed | Normal | group sequential switches with boolean conditions of "x == a" form | Sergey Smolov | Sergey Smolov | 0.1 |
| 6453 | Retrascope | Task | Closed | Normal | Statement class for grouping CFG nodes | Sergey Smolov | Sergey Smolov | 0.1 |
| 6431 | Retrascope | Task | Closed | Normal | descriptor for (VHDL) variables & signals | Sergey Smolov | Sergey Smolov | 0.1 |
| 6412 | Retrascope | Task | Rejected | Normal | engine combining HLDD & assertion model | Sergey Smolov | Sergey Smolov | 0.1 |
| 6410 | Retrascope | Task | Closed | Normal | no-loop/no-recursion functions elaboration | Sergey Smolov | Sergey Smolov | 0.1 |
| 6389 | Retrascope | Task | Closed | Normal | Wiki documentation about testbench simulation | Sergey Smolov | Sergey Smolov | 0.1 |
| 6327 | Retrascope | Task | Closed | Normal | log messages class | Sergey Smolov | Sergey Smolov | 0.1 |
| 6059 | Retrascope | Task | Closed | Normal | Simple solver for "x && !x" constraints | Sergey Smolov | Sergey Smolov | 0.1 |
| 6051 | Retrascope | Task | Closed | Normal | state-like variable names option | Sergey Smolov | Sergey Smolov | 0.1 |
| 6041 | Retrascope | Task | Closed | Normal | move to gradle based build system | Sergey Smolov | Sergey Smolov | 0.1 |
| 5904 | Retrascope | Task | Closed | Normal | save jUnit test results in build/test-results | Sergey Smolov | Sergey Smolov | 0.1 |
| 5897 | Retrascope | Task | Closed | Normal | fix javadoc for methods using InvariantChecks.checkNotNull | Sergey Smolov | Sergey Smolov | 0.1 |
| 5896 | Retrascope | Task | Closed | Normal | remove parameterized collections from public method interfaces | Sergey Smolov | Sergey Smolov | 0.1 |
| 5875 | Retrascope | Task | Closed | Normal | Check state/transition count for extracted EFSM models | Sergey Smolov | Sergey Smolov | 0.1 |
| 5872 | Retrascope | Task | Closed | Normal | HDL file meta info | Sergey Smolov | Sergey Smolov | 0.1 |
| 5868 | Retrascope | Task | Closed | Normal | Migrate to Fortress 0.4 | Sergey Smolov | Sergey Smolov | 0.1 |
| 5832 | Retrascope | Task | Closed | Normal | print some info about failed tests | Sergey Smolov | Sergey Smolov | 0.1 |
| 5756 | Retrascope | Task | Closed | Normal | EFSM pre-initial state + initialization action | Sergey Smolov | Sergey Smolov | 0.1 |

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| 5755 | Retrascope | Task | Closed | Low | use Zamia IG visitors & walkers | Sergey Smolov | Sergey Smolov | 0.1 |
| 5704 | Retrascope | Task | Closed | Normal | try to find a way to remove 'toplevel' option | Sergey Smolov | Sergey Smolov | 0.1 |
| 5696 | Retrascope | Task | Closed | Normal | exclude sandbox & test folder from distribution | Sergey Smolov | Sergey Smolov | 0.1 |
| 5695 | Retrascope | Task | Closed | Normal | mark retrascope.sh as executable automatically | Sergey Smolov | Sergey Smolov | 0.1 |
| 5694 | Retrascope | Task | Closed | Normal | collect the *.smt2 files and analyse constraints | Sergey Smolov | Sergey Smolov | 0.1 |
| 5683 | Retrascope | Task | Closed | Normal | STD_LOGIC/STD_ULOGIC processing | Sergey Smolov | Sergey Smolov | 0.1 |
| 5609 | Retrascope | Task | Rejected | Normal | make process-local variables be efsm-model-global | Sergey Smolov | Sergey Smolov | 0.1 |
| 5592 | Retrascope | Task | Closed | Normal | [project] prepare tar.gz distribution for future release | Sergey Smolov | Sergey Smolov | 0.1 |
| 5591 | Retrascope | Task | Closed | Normal | [project] run scripts for Unix/Windows | Sergey Smolov | Sergey Smolov | 0.1 |
| 5590 | Retrascope | Task | Closed | Normal | [efsm][extraction] implement an EFSM initial state & 'reset' signal heuristics | Sergey Smolov | Sergey Smolov | 0.1 |
| 5589 | Retrascope | Task | Closed | Normal | [efsm][extraction] state-like variables use/def statistics | Sergey Smolov | Sergey Smolov | 0.1 |
| 5579 | Retrascope | Task | Closed | Normal | [cfg] simplify the Assignment class | Sergey Smolov | Sergey Smolov | 0.1 |
| 5570 | Retrascope | Task | Closed | Low | [build] build.xml: extract equal code parts from 'test'/'test.short' targets | Sergey Smolov | Sergey Smolov | 0.1 |
| 5569 | Retrascope | Task | Closed | Normal | support process variable declarations | Sergey Smolov | Sergey Smolov | 0.1 |
| 5568 | Retrascope | Task | Closed | Normal | [cfg] support process variable declarations | Sergey Smolov | Sergey Smolov | 0.1 |
| 5561 | Retrascope | Task | Closed | Normal | [project] use InvariantChecks if needed | Sergey Smolov | Sergey Smolov | 0.1 |
| 5507 | Retrascope | Task | Rejected | Normal | [engine][basis] implement PrinterEngine | Sergey Smolov | Sergey Smolov | 0.1 |
| 5503 | Retrascope | Task | Closed | Normal | [parser][basis][backend] implement "atomic hammock" backend | Sergey Smolov | Sergey Smolov | 0.1 |
| 5482 | Retrascope | Task | Closed | Normal | [wiki] documentation for 0.1-alpha | Sergey Smolov | Sergey Smolov | 0.1 |
| 5481 | Retrascope | Task | Closed | Normal | [structure] remove raw packages from main build folder | Sergey Smolov | Sergey Smolov | 0.1 |
| 5459 | Retrascope | Task | Closed | Normal | implement EngineFrontend/EngineBackend | Sergey Smolov | Sergey Smolov | 0.1 |
| 5446 | Retrascope | Task | Closed | Normal | [efsm][examples] Добавить мета-информацию в B04/B13 | Sergey Smolov | Sergey Smolov | 0.1 |
| 5416 | Retrascope | Task | Closed | Normal | [model][basis] мета-информация | Sergey Smolov | Sergey Smolov | 0.1 |
| 5413 | Retrascope | Task | Closed | High | [model][basis] add HdlType field to VariableData class | Sergey Smolov | Sergey Smolov | 0.1 |
| 5394 | Retrascope | Task | Closed | High | [cgaa][transformer][efsm] реализовать построение переходов EFSM | Sergey Smolov | Sergey Smolov | 0.1 |
| 5226 | Retrascope | Task | Closed | Normal | [cfg][printer][graphml] Узлы SOURCE и BASIC_BLOCK имеют одинаковый цвет | Sergey Smolov | Sergey Smolov | 0.1 |
| 5157 | Retrascope | Task | Closed | Normal | [cfg] addNewVariable(DataType type) | Sergey Smolov | Sergey Smolov | 0.1 |
| 5145 | Retrascope | Task | Closed | Normal | [testbench] Iface | Sergey Smolov | Sergey Smolov | 0.1 |
| 5143 | Retrascope | Task | Closed | Normal | [cfg][extractor][iface] CfgIfaceExtractor | Sergey Smolov | Sergey Smolov | 0.1 |
| 5142 | Retrascope | Task | Closed | Normal | [wiki] Классификация Engine | Sergey Smolov | Sergey Smolov | 0.1 |
| 5117 | Retrascope | Task | Closed | Normal | [parser][basis][backend] CfgMergeBackend | Sergey Smolov | Sergey Smolov | 0.1 |
| 5116 | Retrascope | Task | Closed | Normal | [parser][basis][backend] CfgBasicBlockBackend | Sergey Smolov | Sergey Smolov | 0.1 |

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| 5108 | Retrascope | Task | Closed | Normal | [parser] Реализовать базовые классы Parser, Frontend, Backend | Sergey Smolov | Sergey Smolov | 0.1 |
| 5107 | Retrascope | Task | Closed | Normal | [cfg] Реализовать VhdlExpressionPrinter | Sergey Smolov | Sergey Smolov | 0.1 |
| 5095 | Retrascope | Task | Closed | Normal | [parser][cfg] Оптимизация представления ветвлений - многовариантные узлы switch | Sergey Smolov | Sergey Smolov | 0.1 |
| 5090 | Retrascope | Task | Closed | Normal | [cfg] Оптимизация представления ветвлений | Sergey Smolov | Sergey Smolov | 0.1 |
| 4999 | Retrascope | Task | Closed | Normal | [cfg][transformer][cgaa] CFG-to-GADD transformer | Sergey Smolov | Sergey Smolov | 0.1 |
| 4998 | Retrascope | Task | Closed | Normal | [model][cgaa] Data structure for guarded actions decision diagram | Sergey Smolov | Sergey Smolov | 0.1 |
| 4984 | Retrascope | Task | Closed | Normal | [vhdl][translator] Группировка неблокирующих присваиваний | Sergey Smolov | Sergey Smolov | 0.1 |
| 4972 | Retrascope | Task | Closed | Normal | [model][cgaa] странное расположение метода addVarNamePrefix | Sergey Smolov | Sergey Smolov | 0.1 |
| 4971 | Retrascope | Task | Rejected | Normal | [model][basis] AssignAtomicStatement vs Binding | Sergey Smolov | Sergey Smolov | 0.1 |
| 4967 | Retrascope | Task | Closed | Normal | [model][basis] Реализовать хранилище деклараций переменных | Sergey Smolov | Sergey Smolov | 0.1 |
| 4966 | Retrascope | Task | Closed | Normal | [model][basis] Убрать поле isDefined класса MVariableData | Sergey Smolov | Sergey Smolov | 0.1 |
| 4927 | Retrascope | Task | Rejected | Normal | [cfg][model] Убрать узел типа ASSERT | Sergey Smolov | Sergey Smolov | 0.1 |
| 4925 | Retrascope | Task | Closed | Normal | [vhdl][translator] Обработка непрерывных присваиваний | Sergey Smolov | Sergey Smolov | 0.1 |
| 4924 | Retrascope | Task | Closed | Normal | [cfg][model] Представление непрерывных присваиваний | Sergey Smolov | Sergey Smolov | 0.1 |
| 4829 | Retrascope | Task | Closed | Normal | [cfg][transformer][cgaa] CFG: Assertion building | Sergey Smolov | Sergey Smolov | 0.1 |
| 4558 | Retrascope | Task | Closed | Normal | [cfg][model] Реализовать обходчик для внутреннего представления описаний аппаратуры | Sergey Smolov | Sergey Smolov | 0.1 |
| 9823 | Retrascope IDE | Task | Verified | Normal | README.txt -> README | Sergey Smolov | Maxim Chudnov | 0.1 |
| 9815 | Retrascope IDE | Task | New | Normal | uninstaller for Retrascope IDE | Sergey Smolov | Maxim Chudnov | 0.1 |
| 9810 | Retrascope IDE | Task | New | Normal | Gradle build system | Sergey Smolov | Maxim Chudnov | 0.1 |
| 9776 | Retrascope IDE | Task | Verified | Normal | try to use SVEditor instead of veditor | Sergey Smolov | Maxim Chudnov | 0.1 |
| 9764 | Retrascope IDE | Task | New | High | migrate to Eclipse 2019 | Sergey Smolov | Maxim Chudnov | 0.1 |
| 6988 | Retrascope IDE | Task | New | Normal | [efsm][visualizator][zest] "organic" layout for EFSM models | Sergey Smolov | Maxim Chudnov | 0.1 |
| 5702 | Retrascope IDE | Task | New | Normal | [tool] create Retrascope icon | Sergey Smolov | Maxim Chudnov | 0.1 |
| 5546 | Retrascope IDE | Task | New | Normal | [log] print Retrascope log to Eclipse log | Sergey Smolov | Maxim Chudnov | 0.1 |
| 5251 | Retrascope IDE | Task | New | Normal | [tool][configurator] Сохранение конфигураций | Sergey Smolov | Maxim Chudnov | 0.1 |
| 6990 | Retrascope IDE | Task | Rejected | Normal | use veditor 1.2.1c | Sergey Smolov | Sergey Smolov | 0.1 |
| 6989 | Retrascope IDE | Task | Rejected | Normal | migrate to Eclipse Mars (4.5) | Sergey Smolov | Sergey Smolov | 0.1 |
| 6983 | Retrascope IDE | Task | Closed | Normal | [cfg][visualizator][zest] visualize CfgAssertStatement & CfgLoopStatement nodes | Sergey Smolov | Sergey Smolov | 0.1 |
| 9888 | Retrascope IDE | Task | New | Normal | complete migration from Ant to Gradle build system | Sergey Smolov | | 0.1 |
| 10018 | Trace Matcher | Task | Closed | Normal | migrate to Python 3 | Sergey Smolov | Sergey Smolov | 0.1 |
| 10017 | Trace Matcher | Task | Closed | Normal | README\ChangeLog -> README.md\ChangeLog.md | Sergey Smolov | Sergey Smolov | 0.1 |
| 10016 | Trace Matcher | Task | Closed | Normal | Use Gradle 4.10.3 in build system | Sergey Smolov | Sergey Smolov | 0.1 |

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| 8432 | Trace Matcher | Task | Closed | Normal | register records: register names can contain all but space symbols | Sergey Smolov | Sergey Smolov | 0.1 |
| 8184 | Trace Matcher | Task | Closed | Normal | compare record fields in case insensitive mode | Sergey Smolov | Sergey Smolov | 0.1 |
| 8181 | Trace Matcher | Task | Closed | Normal | check whether trace records are ordered by time | Sergey Smolov | Sergey Smolov | 0.1 |
| 8179 | Trace Matcher | Task | Closed | Normal | ChangeLog | Sergey Smolov | Sergey Smolov | 0.1 |
| 8161 | Trace Matcher | Task | Closed | Normal | Basic modules | Sergey Smolov | Sergey Smolov | 0.1 |
| 8113 | Trace Matcher | Task | Closed | Normal | Gradle build environment | Sergey Smolov | Sergey Smolov | 0.1 |
| 7733 | Trace Matcher | Task | Closed | Normal | run.bat script for Windows | Sergey Smolov | Sergey Smolov | 0.1 |
| 7732 | Trace Matcher | Task | Closed | Normal | oracle: record queue based comparison approach | Sergey Smolov | Sergey Smolov | 0.1 |
| 7663 | Trace Matcher | Task | Closed | Normal | "main" function | Sergey Smolov | Sergey Smolov | 0.1 |
| 9999 | Castle | Task | Closed | Normal | ChangeLog -> ChangeLog.md | Sergey Smolov | Sergey Smolov | 0.1 |
| 9998 | Castle | Task | Closed | Normal | README -> README.md | Sergey Smolov | Sergey Smolov | 0.1 |
| 9971 | MicroTESK for RISC-V | Task | Closed | Normal | print Spike trace to separate log file for every JUnit test case | Sergey Smolov | Sergey Smolov | 0.1 |
| 9811 | Verilog Translator | Task | Closed | High | macro with parameters | Sergey Smolov | Alexey Danilov | 0.2 |
| 6393 | Retrascope | Task | Rejected | Normal | migrate to EFSM model containing only concurrent assignments | Sergey Smolov | Igor Melnichenko | 0.2 |
| 6447 | Retrascope | Task | Closed | Normal | SMV-based counterexamples parser | Sergey Smolov | Mikhail Lebedev | 0.2 |
| 8293 | Retrascope | Task | Closed | Normal | add VeriTrans & Fortress info to NOTICE | Sergey Smolov | Sergey Smolov | 0.2 |
| 8288 | Retrascope | Task | Closed | Normal | use DFS_NO_RPT walking where it is possible | Sergey Smolov | Sergey Smolov | 0.2 |
| 8194 | Retrascope | Task | Closed | Normal | Separately solve independent sub-expressions of common AND expression | Sergey Smolov | Sergey Smolov | 0.2 |
| 7972 | Retrascope | Task | Closed | Normal | empty event-free cases merging backend | Sergey Smolov | Sergey Smolov | 0.2 |
| 7906 | Retrascope | Task | Closed | Normal | Backend that merges "neighbour ranged" sequential 'if' statements | Sergey Smolov | Sergey Smolov | 0.2 |
| 7806 | Retrascope | Task | Closed | Normal | [cgaa] process - collection of diagrams | Sergey Smolov | Sergey Smolov | 0.2 |
| 7742 | Retrascope | Task | Closed | Normal | enum support | Sergey Smolov | Sergey Smolov | 0.2 |
| 7727 | Retrascope | Task | Closed | Normal | Flatten module instances | Sergey Smolov | Sergey Smolov | 0.2 |
| 7715 | Retrascope | Task | Closed | Normal | [refactoring] duplicate code in AssertionVariableContainer | Sergey Smolov | Sergey Smolov | 0.2 |
| 7626 | Retrascope | Task | Closed | Normal | HDL Retrascope 0.2.2-beta release | Sergey Smolov | Sergey Smolov | 0.2 |
| 7623 | Retrascope | Task | Closed | Normal | HLDD-to-SMV printer with no assertions | Sergey Smolov | Sergey Smolov | 0.2 |
| 7597 | Retrascope | Task | Closed | Normal | EfsmTransition.getGuardedAction().getGuard() -> EfsmTransition.getGuard() | Sergey Smolov | Sergey Smolov | 0.2 |
| 7595 | Retrascope | Task | Closed | Normal | GuardedAction.getGuard().getNode() -> GuardedAction.getGuardNode() | Sergey Smolov | Sergey Smolov | 0.2 |
| 7574 | Retrascope | Task | Closed | Normal | Efsm: deepCopy() | Sergey Smolov | Sergey Smolov | 0.2 |
| 7546 | Retrascope | Task | Closed | Normal | Print tool execution time in milliseconds | Sergey Smolov | Sergey Smolov | 0.2 |
| 7409 | Retrascope | Task | Closed | Normal | EFSM state abstraction (stabilization) | Sergey Smolov | Sergey Smolov | 0.2 |

| # | Project | Tracker | Status | Priority | Subject | Author | Assignee | Target version |
|---|---|---|---|---|---|---|---|---|
| 7271 | Retrascope | Task | Closed | Normal | add javadoc for new methods when efsm.state.abstraction branch will be merged into master | Sergey Smolov | Sergey Smolov | 0.2 |
| 7104 | Retrascope | Task | Closed | High | smv-test-parser: filter tests | Sergey Smolov | Sergey Smolov | 0.2 |
| 7096 | Retrascope | Task | Closed | Normal | assign process merging backend | Sergey Smolov | Sergey Smolov | 0.2 |
| 7081 | Retrascope | Task | Rejected | Normal | xor-composition-printer | Sergey Smolov | Sergey Smolov | 0.2 |
| 6976 | Retrascope | Task | Closed | Normal | Wiki update | Sergey Smolov | Sergey Smolov | 0.2 |
| 6956 | Retrascope | Task | Closed | Normal | HDL Retrascope 0.2.1 release | Sergey Smolov | Sergey Smolov | 0.2 |
| 6808 | Retrascope | Task | Rejected | High | Split CFG processes into independent parts | Sergey Smolov | Sergey Smolov | 0.2 |
| 6758 | Retrascope | Task | Closed | Normal | return state/transition coverage for the specified EFSM & test entities | Sergey Smolov | Sergey Smolov | 0.2 |
| 6060 | Retrascope | Task | Closed | Normal | Add plasma to project test suite | Sergey Smolov | Sergey Smolov | 0.2 |
| 5689 | Retrascope | Task | Closed | High | implement test-to-Verilog printer | Sergey Smolov | Sergey Smolov | 0.2 |
| 5549 | Retrascope | Task | Closed | Normal | [vhdl][cfg][parser] add support of instantiation | Sergey Smolov | Sergey Smolov | 0.2 |
| 5548 | Retrascope | Task | Closed | Low | elaborate minimips modules | Sergey Smolov | Sergey Smolov | 0.2 |
| 5395 | Retrascope | Task | Closed | Normal | [cfg] getOnlyChild(), getOnlyParent() | Sergey Smolov | Sergey Smolov | 0.2 |
| 5322 | Retrascope | Task | Closed | Normal | [cgaa][transformer][efsm] Продумать и реализовать эвристику определения reset | Sergey Smolov | Sergey Smolov | 0.2 |
| 5320 | Retrascope | Task | Rejected | Normal | [cfg] Методы копирования вершин CFG | Sergey Smolov | Sergey Smolov | 0.2 |
| 5175 | Retrascope | Task | Closed | Normal | [vhdl][parser] IG array elaboration | Sergey Smolov | Sergey Smolov | 0.2 |
| 5161 | Retrascope | Task | Closed | Normal | [parser][cfg] Обработка циклов | Sergey Smolov | Sergey Smolov | 0.2 |
| 5122 | Retrascope | Task | Closed | Normal | [parser][backend] elaborate non-blocking assignments | Sergey Smolov | Sergey Smolov | 0.2 |
| 4929 | Retrascope | Task | Rejected | Normal | [cfg][model] Добавить структуру данных для представления задержек (delay) в присваиваниях | Sergey Smolov | Sergey Smolov | 0.2 |
| 4466 | Retrascope | Task | Closed | Normal | [vhdl][parser][cfg] преобразование IGSequentialWait | Sergey Smolov | Sergey Smolov | 0.2 |
| 9363 | QEMU4V | Task | Closed | Normal | remove 'set_q4v_tstamp' function calls from RISC-V/MIPS/Aarch64 'cpu_loop.c' modules | Sergey Smolov | Sergey Smolov | 0.2 |
| 9269 | QEMU4V | Task | Closed | Normal | migrate to QEMU 3.0.0 | Sergey Smolov | Sergey Smolov | 0.2 |
| 4702 | Fortress | Task | Closed | Normal | [expression] Реализовать операцию BVBIT | Sergey Smolov | Alexander Kamkin | 0.3 |
| 5907 | Fortress | Task | Closed | Normal | boolean areOfType(DataTypeId id, Node ... nodes) | Sergey Smolov | Andrei Tatarnikov | 0.3 |
| 5861 | Fortress | Task | Closed | Low | static boolean containsSingleObject(Collection<?> collection) | Sergey Smolov | Andrei Tatarnikov | 0.3 |
| 5802 | Fortress | Task | Closed | High | NodeValue newZero(DataType dataType) | Sergey Smolov | Andrei Tatarnikov | 0.3 |
| 5599 | Fortress | Task | Closed | Normal | [expression] implement getDataTypeId() method | Sergey Smolov | Andrei Tatarnikov | 0.3 |
| 5576 | Fortress | Task | Closed | Normal | Calculate data type of expression with BVCONCAT | Sergey Smolov | Andrei Tatarnikov | 0.3 |
| 5563 | Fortress | Task | Closed | Normal | [data] implement DataTypeId.isLogic(Enum<?> id) method | Sergey Smolov | Andrei Tatarnikov | 0.3 |
| 5466 | Fortress | Task | Closed | High | [solver] print the input constraint when solver returns ERROR/UNKNOWN verdict | Sergey Smolov | Andrei Tatarnikov | 0.3 |
| 5465 | Fortress | Task | Closed | Normal | [z3][solver] solver errors elaboration scheme | Sergey Smolov | Andrei Tatarnikov | 0.3 |
| 5464 | Fortress | Task | Closed | High | [solver] boolean expressions casting into bit vectors | Sergey Smolov | Andrei Tatarnikov | 0.3 |

| # | Project | Tracker | Status | Priority | Subject | Author | Assignee | Target version |
|---|---|---|---|---|---|---|---|---|
| 5399 | Fortress | Task | Closed | Normal | silent & debug mode | Sergey Smolov | Andrei Tatarnikov | 0.3 |
| 5319 | Fortress | Task | Closed | Low | [expression] Реализовать метод получения коллекции NodeVariable по объекту Node | Sergey Smolov | Andrei Tatarnikov | 0.3 |
| 5318 | Fortress | Task | Closed | Low | [solver][expression] Реализовать метод разрешения ограничений  SolverResult solve(Constraint constraint) | Sergey Smolov | Andrei Tatarnikov | 0.3 |
| 5317 | Fortress | Task | Closed | Low | [expression] Реализовать метод построения Constraint по Node | Sergey Smolov | Andrei Tatarnikov | 0.3 |
| 5316 | Fortress | Task | Closed | Low | [expression] Операции теории множеств над коллекциями объектов Node | Sergey Smolov | Andrei Tatarnikov | 0.3 |
| 5313 | Fortress | Task | Closed | Normal | [expression] Сделать публичным метод ExprUtils.isSAT(Node assertion) | Sergey Smolov | Andrei Tatarnikov | 0.3 |
| 5259 | Fortress | Task | Rejected | Normal | [build] удаление папки distr при выполнении команды ant clean | Sergey Smolov | Andrei Tatarnikov | 0.3 |
| 4802 | Fortress | Task | Closed | Normal | [solver][constraint] создание Constraint без указания variables | Sergey Smolov | Andrei Tatarnikov | 0.3 |
| 4699 | Fortress | Task | Closed | Normal | [data][solver] поддержка массивов SMT-LIB | Sergey Smolov | Andrei Tatarnikov | 0.3 |
| 4554 | Fortress | Task | Closed | Normal | [solver][xml] Метод преобразования ограничения в XML-based String | Sergey Smolov | Andrei Tatarnikov | 0.3 |
| 5600 | Fortress | Task | Closed | High | [transformer][ruleset] implement ITE rules | Sergey Smolov | Artem Kotsynyak | 0.3 |
| 5462 | Fortress | Task | Closed | Normal | [arrays] arrays initialization is inconvenient | Sergey Smolov | Artem Kotsynyak | 0.3 |
| 5447 | Fortress | Task | Closed | High | [transformer][ruleset] стандартизация константных выражений вида "x EQ y" | Sergey Smolov | Artem Kotsynyak | 0.3 |
| 5433 | Fortress | Task | Closed | Normal | [test] write executable SMT-LIB code at testcase comments | Sergey Smolov | Artem Kotsynyak | 0.3 |
| 5424 | Fortress | Task | Closed | High | [transformer][ruleset] дополнительные правила стандартизации | Sergey Smolov | Artem Kotsynyak | 0.3 |
| 5419 | Fortress | Task | Closed | High | [transformer][ruleset] реализовать правило expr==false -> NOT(expr == true) | Sergey Smolov | Artem Kotsynyak | 0.3 |
| 5229 | Fortress | Task | Closed | High | [transformer] Упрощение выражений с LOGIC_BOOLEAN | Sergey Smolov | Artem Kotsynyak | 0.3 |
| 4673 | Fortress | Task | Closed | Normal | [solver][constraint] Ограничения без имен | Sergey Smolov | Sergey Smolov | 0.3 |
| 4671 | Fortress | Task | Closed | Normal | [data] Метод построения битовых векторов из их строкового представления | Sergey Smolov | Sergey Smolov | 0.3 |
| 9373 | QEMU4V | Task | Closed | Normal | write a PowerPC-related chapter to "Getting Started" | Sergey Smolov | Maxim Chudnov | 0.3 |
| 10611 | QEMU4V | Task | Resolved | Normal | migrate to QEMU 5.2.0 | Sergey Smolov | Sergey Smolov | 0.3 |
| 10474 | QEMU4V | Task | Resolved | Normal | migrate to QEMU 5.1.0 | Sergey Smolov | Sergey Smolov | 0.3 |
| 10258 | QEMU4V | Task | Closed | Normal | migrate to QEMU 5.0 | Sergey Smolov | Sergey Smolov | 0.3 |
| 9986 | QEMU4V | Task | New | Normal | check if QEMU4V features can be implemented as TCG plugin | Sergey Smolov | Sergey Smolov | 0.3 |
| 9917 | QEMU4V | Task | Closed | Normal | check QEMU4V-specific code on compliance with coding style | Sergey Smolov | Sergey Smolov | 0.3 |
| 9909 | QEMU4V | Task | Closed | Normal | migrate to QEMU 4.2.0 | Sergey Smolov | Sergey Smolov | 0.3 |
| 9863 | QEMU4V | Task | Closed | Normal | use Gradle 4.10.3 | Sergey Smolov | Sergey Smolov | 0.3 |
| 9862 | QEMU4V | Task | Closed | Normal | migrate to QEMU 4.1.0 | Sergey Smolov | Sergey Smolov | 0.3 |
| 9415 | QEMU4V | Task | Closed | Normal | migrate to QEMU 3.1.0 | Sergey Smolov | Sergey Smolov | 0.3 |
| 7561 | Fortress | Task | New | Normal | ISampleConstraint: 'getExpectedVariables' returns value that is ignored in jUnit tests | Sergey Smolov | Andrei Tatarnikov | 0.4 |
| 7402 | Fortress | Task | Closed | Normal | ExprUtils: ignore repeated Node objects upon conjunction/disjunction construction | Sergey Smolov | Andrei Tatarnikov | 0.4 |
| 7397 | Fortress | Task | Closed | Normal | NodeVariable.new<type-of-variable>(final String name) | Sergey Smolov | Andrei Tatarnikov | 0.4 |

| # | Project | Tracker | Status | Priority | Subject | Author | Assignee | Target version |
|---|---|---|---|---|---|---|---|---|
| 7383 | Fortress | Task | Closed | Normal | boolean isOperation(final Node expr, final T... opId) | Sergey Smolov | Andrei Tatarnikov | 0.4 |
| 6423 | Fortress | Task | Rejected | Low | to_real, to_int, is_int operations | Sergey Smolov | Andrei Tatarnikov | 0.4 |
| 6364 | Fortress | Task | Rejected | Low | SolverResult: implement equals\hashcode methods | Sergey Smolov | Andrei Tatarnikov | 0.4 |
| 5993 | Fortress | Task | Closed | Normal | boolean ExprUtils.isKind(Node.Kind kind, Node ... nodes) | Sergey Smolov | Andrei Tatarnikov | 0.4 |
| 5985 | Fortress | Task | Closed | High | Node ExprUtils.getEquation(Node target, Node value) | Sergey Smolov | Andrei Tatarnikov | 0.4 |
| 7378 | Fortress | Task | Closed | Low | NodeTransformer: multiple transform rules for a single enum id | Sergey Smolov | Artem Kotsynyak | 0.4 |
| 6831 | Fortress | Task | Closed | Normal | ESExprParser: improve error messages | Sergey Smolov | Artem Kotsynyak | 0.4 |
| 5478 | Fortress | Task | Closed | Normal | Implement Transformer.reduce(Node expression) | Sergey Smolov | Artem Kotsynyak | 0.4 |
| 4713 | Fortress | Task | New | High | SMT-LIB structures | Sergey Smolov | Artem Kotsynyak | 0.4 |
| 10494 | Fortress | Task | Closed | Normal | check Windows build of Boolector on project tests | Sergey Smolov | Maxim Chudnov | 0.4 |
| 10492 | Fortress | Task | Closed | Normal | use CVC4 1.8 in testing | Sergey Smolov | Sergey Smolov | 0.4 |
| 10002 | Fortress | Task | Closed | Normal | get Boolector solver from server as dependency | Sergey Smolov | Sergey Smolov | 0.4 |
| 7772 | Fortress | Task | Closed | High | TypeConversion.coerce: transform from MAP to BIT_VECTOR | Sergey Smolov | Sergey Smolov | 0.4 |
| 7527 | Fortress | Task | Closed | Normal | constant casting while type conversion | Sergey Smolov | Sergey Smolov | 0.4 |
| 7846 | Fortress | Task | Rejected | Normal | 'Transformer.reduce(Transformer.substitute(expression, name, term))' convenience method | Sergey Smolov | | 0.4 |
| 9766 | Retrascope | Task | Closed | High | remove 'vhdl.record' Git branch from remote repo | Sergey Smolov | Maxim Chudnov | 1.0 |
| 9658 | Retrascope | Task | Closed | Normal | Check for duplicated data access conflict assertions | Sergey Smolov | Mikhail Lebedev | 1.0 |
| 9280 | Retrascope | Task | Closed | Normal | prepare the code to 1.1.1 release | Sergey Smolov | Mikhail Lebedev | 1.0 |
| 9278 | Retrascope | Task | Closed | Normal | use CGAA model instead of EFSM-based assertions to get clocks | Sergey Smolov | Mikhail Lebedev | 1.0 |
| 6472 | Retrascope | Task | Closed | Normal | b13.vhd: too long elaboration time | Sergey Smolov | Mikhail Lebedev | 1.0 |
| 5711 | Retrascope | Task | Closed | Normal | Check generated *.smv files with external model checker | Sergey Smolov | Mikhail Lebedev | 1.0 |
| 9806 | Retrascope | Task | Closed | Normal | rm dependency from commons-lang library | Sergey Smolov | Sergey Smolov | 1.0 |
| 9762 | Retrascope | Task | Closed | High | prepare to 1.1.1 release | Sergey Smolov | Sergey Smolov | 1.0 |
| 9484 | Retrascope | Task | Closed | Normal | Check variables\switches\basic blocks number at HDL parser test cases | Sergey Smolov | Sergey Smolov | 1.0 |
| 9462 | Retrascope | Task | Closed | Normal | jUnit test cases for HDL parsers that count numbers of CFG processes, statements, etc. | Sergey Smolov | Sergey Smolov | 1.0 |
| 9438 | Retrascope | Task | Closed | Normal | jUnit test cases for CFG-GAD transformer that check path number | Sergey Smolov | Sergey Smolov | 1.0 |
| 9430 | Retrascope | Task | Closed | Normal | CGAA -> GADD | Sergey Smolov | Sergey Smolov | 1.0 |
| 9427 | Retrascope | Task | Closed | Normal | reuse variables' versions upon CGAA model building | Sergey Smolov | Sergey Smolov | 1.0 |
| 9389 | Retrascope | Task | Closed | Normal | Assertion -> Property | Sergey Smolov | Sergey Smolov | 1.0 |
| 9310 | Retrascope | Task | Closed | Normal | substitute SMT-LIB variables those names are equal to builtin commands | Sergey Smolov | Sergey Smolov | 1.0 |
| 9291 | Retrascope | Task | Closed | Normal | use nuXmv 1.1.1 | Sergey Smolov | Sergey Smolov | 1.0 |
| 9277 | Retrascope | Task | Closed | High | mv clock-like variable detection to CFG-to-CGAA transformer | Sergey Smolov | Sergey Smolov | 1.0 |

| # | Project | Tracker | Status | Priority | Subject | Author | Assignee | Target version |
|---|---|---|---|---|---|---|---|---|
| 9249 | Retrascope | Task | Closed | Normal | separate jUnit test cases for EfsmGraphMlPrinter engine | Sergey Smolov | Sergey Smolov | 1.0 |
| 9248 | Retrascope | Task | Closed | High | CFG model process should not have it's own internal variables | Sergey Smolov | Sergey Smolov | 1.0 |
| 9242 | Retrascope | Task | Closed | High | check BVEXTRACT operation's parameter order | Sergey Smolov | Sergey Smolov | 1.0 |
| 9196 | Retrascope | Task | Closed | Normal | CfgVarRangeBlockBackend: use array length for assignment elaboration | Sergey Smolov | Sergey Smolov | 1.0 |
| 9191 | Retrascope | Task | Closed | Normal | use StringTemplate facilities to generate HDL testbenches | Sergey Smolov | Sergey Smolov | 1.0 |
| 8994 | Retrascope | Task | Closed | Normal | "BVEXTRACT( ... BVEXTRACT (j i x))" expression transformation rule to the tool ruleset | Sergey Smolov | Sergey Smolov | 1.0 |
| 8976 | Retrascope | Task | Closed | Normal | Range: old -> high, young -> low | Sergey Smolov | Sergey Smolov | 1.0 |
| 8975 | Retrascope | Task | Closed | Normal | RetrascopeException.makeException -> RetrascopeException.exception | Sergey Smolov | Sergey Smolov | 1.0 |
| 8430 | Retrascope | Task | Closed | Normal | meta-info type for CFG statements that were added by HDL parser backends | Sergey Smolov | Sergey Smolov | 1.0 |
| 8429 | Retrascope | Task | Closed | Normal | backend that transforms "x[i] := y" assignments into constant-ranged | Sergey Smolov | Sergey Smolov | 1.0 |
| 7770 | Retrascope | Task | Closed | Normal | 'others' attribute upon array/bitvector initialization | Sergey Smolov | Sergey Smolov | 1.0 |
| 7723 | Retrascope | Task | Rejected | Normal | Support for module instances in Verilog descriptions | Sergey Smolov | Sergey Smolov | 1.0 |
| 6301 | Retrascope | Task | Closed | Normal | unused code | Sergey Smolov | Sergey Smolov | 1.0 |
| 6061 | Retrascope | Task | Closed | Normal | EFSM-based transition assertion generator | Sergey Smolov | Sergey Smolov | 1.0 |
| 5588 | Retrascope | Task | Closed | Normal | extend HDL test suite | Sergey Smolov | Sergey Smolov | 1.0 |
| 10139 | Retrascope | Task | Verified | High | fix coding issues at *BenchTest classes | Sergey Smolov | Maxim Chudnov | 1.1 |
| 10128 | Retrascope | Task | Verified | Normal | rename multi-test classes: "*TestCase" -> "*TestSuite" | Sergey Smolov | Maxim Chudnov | 1.1 |
| 10073 | Retrascope | Task | Verified | High | fix checkstyle warnings | Sergey Smolov | Maxim Chudnov | 1.1 |
| 10059 | Retrascope | Task | Rejected | Normal | mv all the project tests to JUnit 5 platform | Sergey Smolov | Maxim Chudnov | 1.1 |
| 9911 | Retrascope | Task | Verified | Urgent | merge "*/sample/*TestCase" Java test cases | Sergey Smolov | Maxim Chudnov | 1.1 |
| 10133 | Retrascope | Task | New | Normal | use '-coi' model checker option | Sergey Smolov | Mikhail Lebedev | 1.1 |
| 10166 | Retrascope | Task | Resolved | Normal | rename some class fields & related methods | Sergey Smolov | Sergey Smolov | 1.1 |
| 10000 | Retrascope | Task | Verified | Normal | README\ChangeLog -> README.md\ChangeLog.md | Sergey Smolov | Sergey Smolov | 1.1 |
| 9964 | Retrascope | Task | Verified | Normal | add HDL examples to project distribution | Sergey Smolov | Sergey Smolov | 1.1 |
| 5504 | Retrascope | Task | New | Normal | add channels between EFSMs | Sergey Smolov | Mikhail Lebedev | 1.2 |
| 10058 | Retrascope | Task | New | Normal | User documentation | Sergey Smolov | Sergey Smolov | 1.2 |
| 9488 | Retrascope | Task | New | Normal | CFG-GADD transformer backend that makes assignments index and range-free | Sergey Smolov | Sergey Smolov | 1.2 |
| 6446 | Retrascope | Task | New | Normal | Promela translator to CFG representation (no buffers) | Sergey Smolov | Mikhail Lebedev | 2.0 |
| 6449 | Retrascope | Task | New | Low | testbench generator taking test sequences and mappings as inputs | Sergey Smolov | Sergey Smolov | 2.0 |
| 6448 | Retrascope | Task | New | Low | mapping description language + IR + parser | Sergey Smolov | Sergey Smolov | 2.0 |
| 4521 | Retrascope | Task | New | Low | Входной класс для генератора тестовой последовательности | Sergey Smolov | Sergey Smolov | 2.0 |
| 4363 | Retrascope | Task | New | Low | Критерий кластеризации входных сигналов, основанный на GA | Sergey Smolov | Sergey Smolov | 2.0 |

| # | Project | Tracker | Status | Priority | Subject | Author | Assignee | Target version |
|---|---|---|---|---|---|---|---|---|
| 10304 | MicroTESK | Task | New | Normal | deprecation warnings via compilation | Sergey Smolov | Alexander Kamkin | 2.5 |
| 7564 | MicroTESK | Task | Closed | Normal | "How to build MicroTESK" guide for developers in project Wiki | Sergey Smolov | Alexander Kamkin | 2.5 |
| 5526 | Retrascope | Task | Rejected | Normal | Retrascope engines configuration | Sergey Smolov | Alexander Kamkin | |
| 2224 | C++TESK Development Environment | Task | Closed | Normal | Добавить пункт со сведениями о плагине | Sergey Smolov | Alexander Kamkin | |
| 5127 | Retrascope IDE | Task | Rejected | Normal | [cfg][printer][graphml] Интегрировать плагин для yEd | Sergey Smolov | Alexander Protsenko | |
| 3694 | Fortress | Task | Closed | Normal | Операции сравнения битовых векторов | Sergey Smolov | Andrei Tatarnikov | |
| 3716 | C++TESK Development Environment | Task | Closed | Normal | Simple XML dumping\parsing test | Sergey Smolov | asd ert | |
| 3950 | Retrascope | Task | Closed | Normal | Переместить служебные файлы Eclipse | Sergey Smolov | Igor Melnichenko | |
| 9235 | Retrascope Test Suite | Task | Closed | Normal | adapt JUnit components to new interface of ToolTest class | Sergey Smolov | Mikhail Lebedev | |
| 9216 | Retrascope Test Suite | Task | Closed | Normal | remove tests for Verilog Translator from project | Sergey Smolov | Mikhail Lebedev | |
| 9839 | Retrascope Test Suite | Task | Rejected | Normal | scripts for commercial FV tools running | Sergey Smolov | Sergey Smolov | |
| 9726 | Retrascope Test Suite | Task | Closed | Normal | VerilogPrinter test cases | Sergey Smolov | Sergey Smolov | |
| 9670 | Retrascope Test Suite | Task | New | High | add 'ar.v' module to the test suite when SVA support will be implemented | Sergey Smolov | Sergey Smolov | |
| 9607 | Retrascope Test Suite | Task | Closed | Normal | add QUIP 9.0 benchmark | Sergey Smolov | Sergey Smolov | |
| 9606 | Retrascope Test Suite | Task | Closed | Normal | add IWLS 2005 benchmark | Sergey Smolov | Sergey Smolov | |
| 9566 | Retrascope Test Suite | Task | Closed | Normal | tests for Yosys-SMTBMC tool | Sergey Smolov | Sergey Smolov | |
| 9565 | Retrascope Test Suite | Task | Closed | Normal | tests for Verilog2SMV tool | Sergey Smolov | Sergey Smolov | |
| 9564 | Retrascope Test Suite | Task | Closed | Normal | tests for EBMC tool | Sergey Smolov | Sergey Smolov | |
| 6507 | Castle | Task | Closed | Normal | build.gradle: get ANTLR jar from server | Sergey Smolov | Sergey Smolov | |
| 6331 | Retrascope | Task | Closed | Normal | look into unused classes | Sergey Smolov | Sergey Smolov | |
| 4807 | Retrascope | Task | Closed | Normal | Action as interface for BasicBlock, Assertion, Situation | Sergey Smolov | Sergey Smolov | |
| 4580 | Retrascope | Task | Closed | Normal | Поместить проект MiniMIPS в share/vhdl | Sergey Smolov | Sergey Smolov | |
| 4465 | Retrascope | Task | Closed | Normal | Объединение присваиваний в базовых блоках | Sergey Smolov | Sergey Smolov | |

| # | Project | Tracker | Status | Priority | Subject | Author | Assignee | Target version |
|---|---|---|---|---|---|---|---|---|
| 4337 | Retrascope | Task | Closed | Normal | реализовать заглушки для методов преобразования в ограничения | Sergey Smolov | Sergey Smolov | |
| 3957 | Retrascope | Task | Closed | High | DFG to EFSM | Sergey Smolov | Sergey Smolov | |
| 3934 | Retrascope | Task | Closed | Normal | Дополнительные операции | Sergey Smolov | Sergey Smolov | |
| 3895 | Fortress | Task | Closed | Normal | Дополнительные операции Verilog | Sergey Smolov | Sergey Smolov | |
| 3754 | C++TESK Development Environment | Task | Closed | Normal | флаг incomparable в полях сообщений | Sergey Smolov | Sergey Smolov | |
| 3734 | Fortress | Task | Closed | Normal | Операции сравнения для LOGIC-типов | Sergey Smolov | Sergey Smolov | |
| 3721 | Fortress | Task | Closed | Normal | Дополнительные операции | Sergey Smolov | Sergey Smolov | |
| 3708 | Fortress | Task | Closed | Normal | Методы makeNegation, makeConjunction, makeDisjunction класса Constraint | Sergey Smolov | Sergey Smolov | |
| 3654 | C++TESK Development Environment | Task | Closed | High | source code refactoring | Sergey Smolov | Sergey Smolov | |
| 3637 | Retrascope | Task | Closed | Normal | Пространство состояний | Sergey Smolov | Sergey Smolov | |
| 3624 | C++TESK Development Environment | Task | Closed | Normal | XML dumping\parsing | Sergey Smolov | Sergey Smolov | |
| 3623 | C++TESK Development Environment | Task | Closed | Normal | Внутреннее  представление для прототипов тестовых систем | Sergey Smolov | Sergey Smolov | |
| 3434 | Retrascope | Task | Closed | Normal | Извлечение "протоопераций" из Data Flow Graph | Sergey Smolov | Sergey Smolov | |
| 3406 | Retrascope | Task | Closed | Normal | CFG extraction from guarded atomic actions (GAA) set. | Sergey Smolov | Sergey Smolov | |
| 10001 | Fortress | Task | Rejected | Normal | SMT-LIBv2 benchmarks | Sergey Smolov | | |
| 9889 | MicroTESK for Plasma | Task | Resolved | Normal | rm deprecated 'findbugs' plugin from Gradle build script | Sergey Smolov | | |
| 9217 | MicroTESK | Task | Closed | Normal | Use 'ru.ispras.castle.codegen' package classes from Castle | Sergey Smolov | | |
| 8167 | QEMU4V | Task | New | Low | Program flow tracing | Sergey Smolov | | |
| 3759 | C++TESK Development Environment | Task | Feedback | Normal | Разработать демонстрационный пример для структуры соответствия | Sergey Smolov | | |
| 3756 | C++TESK Development Environment | Task | New | Immediate | Генерация C++ кода для модели сообщений | Sergey Smolov | | |
| 3755 | C++TESK Development Environment | Task | New | Normal | namespace name for test system prototypes | Sergey Smolov | | |

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| 3659 | C++TESK Development Environment | Task | New | Normal | Соответствие полей классов сообщений и сигналов HDL-модели | Sergey Smolov | | |
| 6537 | Retrascope | Developer Request | Closed | Normal | Efsm: collection of resetting guarded actions | Sergey Smolov | Igor Melnichenko | 0.1 |
| 5580 | Retrascope | Developer Request | Closed | Normal | [efsm][conflict][extractor][jaxb] can GuardedAction() call at the JaxbGuardedActionAdapter be substituted by something else | Sergey Smolov | Mikhail Lebedev | 0.1 |
| 3979 | Retrascope | Developer Request | Closed | Normal | Реструктурирование проекта | Sergey Smolov | Sergey Smolov | |
| 8874 | Verilog Translator | Feature | Closed | High | mapping from instance variables to their code entries | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9990 | Verilog Translator | Feature | Closed | High | check for variable/net redeclarations | Sergey Smolov | Alexey Danilov | 0.1 |
| 10100 | Trace Matcher | Feature | Resolved | Normal | "--boot-size <num>" command line option | Sergey Smolov | Sergey Smolov | 0.1 |
| 10099 | Trace Matcher | Feature | Resolved | Normal | "--start-addr <hex value>" command line option | Sergey Smolov | Sergey Smolov | 0.1 |
| 10015 | Trace Matcher | Feature | Closed | Normal | Report an error when input file is empty | Sergey Smolov | Sergey Smolov | 0.1 |
| 8433 | Trace Matcher | Feature | Closed | Normal | "--skip-equal" command line option | Sergey Smolov | Sergey Smolov | 0.1 |
| 8206 | Trace Matcher | Feature | Closed | Normal | "--debug" command line option | Sergey Smolov | Sergey Smolov | 0.1 |
| 8199 | Trace Matcher | Feature | Closed | Normal | "ignore-the-rest" command line option | Sergey Smolov | Sergey Smolov | 0.1 |
| 8198 | Trace Matcher | Feature | Closed | Normal | "exit-on-first-divergence" command line option | Sergey Smolov | Sergey Smolov | 0.1 |
| 8197 | Trace Matcher | Feature | Closed | Normal | "matching window in ticks" command line option | Sergey Smolov | Sergey Smolov | 0.1 |
| 8305 | Retrascope | Feature | Closed | Normal | EFSM state limit | Sergey Smolov | Sergey Smolov | 0.2 |
| 8304 | Retrascope | Feature | Rejected | Normal | SLR values number limit | Sergey Smolov | Sergey Smolov | 0.2 |
| 8282 | Retrascope | Feature | Closed | Normal | apply SLV detection heuristic to more than one CGAA path | Sergey Smolov | Sergey Smolov | 0.2 |
| 8262 | Retrascope | Feature | Closed | Normal | phase variable based approach for CFG-CGAA-EFSM optimisation | Sergey Smolov | Sergey Smolov | 0.2 |
| 8220 | Retrascope | Feature | Closed | Normal | BV_INC6 VHDL function support | Sergey Smolov | Sergey Smolov | 0.2 |
| 8866 | QEMU4V | Feature | Closed | Normal | trace generation for MIPS programs | Sergey Smolov | Maxim Chudnov | 0.2 |
| 9079 | QEMU4V | Feature | Closed | Normal | basic support for MIPS32 | Sergey Smolov | Sergey Smolov | 0.2 |
| 9049 | QEMU4V | Feature | Closed | Normal | basic support for MIPS64 emulation | Sergey Smolov | Sergey Smolov | 0.2 |
| 8867 | QEMU4V | Feature | Closed | Normal | trace generation for PowerPC (32bit) programs | Sergey Smolov | Maxim Chudnov | 0.3 |
| 9051 | QEMU4V | Feature | Closed | Normal | basic support for PowerPC emulation | Sergey Smolov | Sergey Smolov | 0.3 |
| 8709 | Fortress | Feature | Closed | Normal | 'public static boolean isOperation(final Node node, final T ... opTypes)' convenience method | Sergey Smolov | Andrei Tatarnikov | 0.4 |
| 8703 | Fortress | Feature | Closed | Normal | 'public static boolean isType(final Node node, final DataType ... types)' convenience method | Sergey Smolov | Andrei Tatarnikov | 0.4 |
| 8702 | Fortress | Feature | Closed | Normal | 'public static NodeValue.newBitVector(final boolean value)' convenience method | Sergey Smolov | Andrei Tatarnikov | 0.4 |
| 8667 | Fortress | Feature | Closed | Normal | Nodes.EQ(Node ... nodes) convenience method | Sergey Smolov | Andrei Tatarnikov | 0.4 |

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| 8665 | Fortress | Feature | Closed | High | Nodes.BVEXTRACT(Node, Node, Node) convenience method | Sergey Smolov | Andrei Tatarnikov | 0.4 |
| 9123 | Fortress | Feature | Closed | High | calculate DataType for 'BVEXTRACT(i, i, x)' NodeOperation objects | Sergey Smolov | Sergey Smolov | 0.4 |
| 8204 | Fortress | Feature | Closed | Normal | solver-specific header for generated SMT2 files | Sergey Smolov | Sergey Smolov | 0.4 |
| 8203 | Fortress | Feature | Closed | Normal | bv2nat\int2bv operations | Sergey Smolov | Sergey Smolov | 0.4 |
| 8260 | Retrascope | Feature | Closed | Normal | VHDL record support (non-aggregate case) | Sergey Smolov | Maxim Chudnov | 1.0 |
| 9503 | Retrascope | Feature | Closed | Normal | when debug option is enabled, pass it to the model checker as well | Sergey Smolov | Mikhail Lebedev | 1.0 |
| 9335 | Retrascope | Feature | Closed | Normal | cgaa-assert-extractor engine | Sergey Smolov | Mikhail Lebedev | 1.0 |
| 9041 | Retrascope | Feature | Closed | Normal | when model checker returns an error, print it's log to the Retrascope output | Sergey Smolov | Mikhail Lebedev | 1.0 |
| 9769 | Retrascope | Feature | Closed | Normal | GraphML printers: make branch values italic | Sergey Smolov | Sergey Smolov | 1.0 |
| 9767 | Retrascope | Feature | Closed | Normal | GraphML printers: use dotted arrows for Module->(Module\| Process) hierarchy dependencies | Sergey Smolov | Sergey Smolov | 1.0 |
| 9486 | Retrascope | Feature | Closed | Normal | HDL parser's init_process backend: calculate initial values if possible | Sergey Smolov | Sergey Smolov | 1.0 |
| 9474 | Retrascope | Feature | Closed | Normal | enable\disable backend parameters for all the engines | Sergey Smolov | Sergey Smolov | 1.0 |
| 9468 | Retrascope | Feature | Closed | Normal | HDL parser backend that removes 'initial' processes | Sergey Smolov | Sergey Smolov | 1.0 |
| 9457 | Retrascope | Feature | Closed | Normal | one more auxiliary path in GADD model for terminal endings | Sergey Smolov | Sergey Smolov | 1.0 |
| 9446 | Retrascope | Feature | Closed | Normal | Debug output file for engines and their backends | Sergey Smolov | Sergey Smolov | 1.0 |
| 9281 | Retrascope | Feature | Closed | Normal | cmdline option that specifies clock variable for CGAA model | Sergey Smolov | Sergey Smolov | 1.0 |
| 9264 | Retrascope | Feature | Closed | Normal | '--disable-backends' cmdline option for HDL parser engine | Sergey Smolov | Sergey Smolov | 1.0 |
| 9227 | Retrascope | Feature | Closed | High | support for 'BVEXTRACT(x y (SELECT z w))' constructions in left hand sides of assigments | Sergey Smolov | Sergey Smolov | 1.0 |
| 9149 | Retrascope | Feature | Closed | Normal | elaborate ranged assignments for bitvector target variables | Sergey Smolov | Sergey Smolov | 1.0 |
| 9039 | Retrascope | Feature | Closed | Normal | Support for designs that assign to variable more than once | Sergey Smolov | Sergey Smolov | 1.0 |
| 8615 | Retrascope | Feature | Closed | Normal | "--no-backends" command line option | Sergey Smolov | Sergey Smolov | 1.0 |
| 10287 | Retrascope | Feature | Verified | Normal | TestModel: keep top level module name & variables | Sergey Smolov | Sergey Smolov | 1.1 |
| 10238 | Retrascope | Feature | Resolved | Normal | VerilogParser: '--library-file' cmdline option | Sergey Smolov | Sergey Smolov | 1.1 |
| 10125 | Retrascope | Feature | Resolved | Normal | '--detailed' option for efsm-graphml-printer engine | Sergey Smolov | Sergey Smolov | 1.1 |
| 10116 | Retrascope | Feature | Resolved | Normal | command line option to check if solvers\model checkers that are used are installed properly | Sergey Smolov | Sergey Smolov | 1.1 |
| 10115 | Retrascope | Feature | Verified | Normal | '--version' command line option | Sergey Smolov | Sergey Smolov | 1.1 |
| 10112 | Retrascope | Feature | Resolved | Normal | '--no-phase' command line option for 'cfg-gadd-transformer' engine | Sergey Smolov | Sergey Smolov | 1.1 |
| 10060 | Retrascope | Feature | Resolved | High | Support SVA properties in CFG model | Sergey Smolov | Sergey Smolov | 1.2 |
| 9247 | Retrascope | Feature | Open | High | CFG-to-C printer | Sergey Smolov | Sergey Smolov | 1.2 |
| 10074 | MicroTESK | Feature | New | Normal | option that stores boot obj at the generated ld script | Sergey Smolov | Alexander Kamkin | 2.5 |
| 8587 | MicroTESK | Feature | New | Normal | ISA subsets | Sergey Smolov | Artem Kotsynyak | 2.5 |
| 9050 | QEMU4V | Feature | Closed | Normal | basic support for i386 emulation | Sergey Smolov | Sergey Smolov | |

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|---|---|---|---|---|---|---|---|---|
| 8871 | QEMU4V | Feature | Closed | Normal | "-print-pte-addr" cmdline option | Sergey Smolov | Sergey Smolov | |
| 8870 | QEMU4V | Feature | Closed | Normal | trace generation for RISC-V programs | Sergey Smolov | Sergey Smolov | |
| 8869 | QEMU4V | Feature | Closed | Normal | trace generation for Aarch64 programs | Sergey Smolov | Sergey Smolov | |
| 8868 | QEMU4V | Feature | Closed | Normal | implement tracer that is activated by "-trace-log" command line option | Sergey Smolov | Sergey Smolov | |
| 10290 | Verilog Translator | Feature | New | Normal | SystemVerilog support | Sergey Smolov | | |
| 10088 | QEMU4V | Feature | New | Low | QEMU4V formatted traces for x86 programs | Sergey Smolov | | |
| 4005 | C++TESK Testing ToolKit | Bug | Rejected | Normal | удалить пустой README | Sergey Smolov | asd ert | 1.0 |
| 4004 | C++TESK Testing ToolKit | Bug | Closed | Normal | Из build'а пропал скрипт install-eclipse-plugin.sh | Sergey Smolov | Sergey Smolov | 1.0 |
| 3590 | C++TESK Testing ToolKit | Bug | Closed | Normal | C++TesK installation fails on OpenSUSE 12.2 x64 | Sergey Smolov | Sergey Smolov | 1.0 |
| 6241 | MicroTESK | Bug | Closed | Normal | Generated assembler files contain tab-only lines | Sergey Smolov | Andrei Tatarnikov | 2.2 |
| 6106 | MicroTESK | Bug | Closed | Normal | zero opcodes for instructions in Tarmac log | Sergey Smolov | Andrei Tatarnikov | 2.2 |
| 7730 | MicroTESK | Bug | Closed | High | [tarmac-logger] missing "<cpu>" tag | Sergey Smolov | Andrei Tatarnikov | 2.4 |
| 9437 | MicroTESK | Bug | Closed | Normal | ru.ispras.microtesk.model.minimips.BufferPreparatorTestCase: QEMU4V crashes with general protection error on this test program | Sergey Smolov | Sergey Smolov | 2.4 |
| 10031 | MicroTESK for PowerPC | Bug | New | Normal | WARNING: An illegal reflective access operation has occurred | Sergey Smolov | Alexander Protsenko | 0.0 |
| 10513 | Verilog Translator | Bug | New | Normal | macOS related line endings at Verilog modules | Sergey Smolov | Alexander Kamkin | 0.1 |
| 10512 | Verilog Translator | Bug | New | Normal | ADDA162H90A_atop.v line 120:47 mismatched input ':' expecting RPAREN | Sergey Smolov | Alexander Kamkin | 0.1 |
| 10510 | Verilog Translator | Bug | New | Normal | ERROR: [Internal] Bit vector sizes do not match: 32 != 2. | Sergey Smolov | Alexander Kamkin | 0.1 |
| 10509 | Verilog Translator | Bug | New | Normal | ERROR: [Internal] 0 must be > 0 | Sergey Smolov | Alexander Kamkin | 0.1 |
| 10508 | Verilog Translator | Bug | New | Normal | ERROR: [Internal] Java heap space | Sergey Smolov | Alexander Kamkin | 0.1 |
| 10505 | Verilog Translator | Bug | New | Normal | ERROR: [Internal] 11 must be within range [0, 1) | Sergey Smolov | Alexander Kamkin | 0.1 |
| 10502 | Verilog Translator | Bug | New | Normal | subbytes.v line 76:13 no viable alternative at input '[' | Sergey Smolov | Alexander Kamkin | 0.1 |
| 10246 | Verilog Translator | Bug | Rejected | Normal | ru.ispras.verilog.parser.VerilogQuipTestSuite#runTest_nut_001: ERROR: Module 'lut_output' has not been found | Sergey Smolov | Alexander Kamkin | 0.1 |

| # | Project | Tracker | Status | Priority | Subject | Author | Assignee | Target version |
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| 10241 | Verilog Translator | Bug | Closed | Normal | ru.ispras.verilog.parser.VerilogQuipTestSuite#runTest_dctub_jpeg: ERROR: ..\src\test\verilog\hdl-benchmarks\hdl\quip\oc_video_compression_systems_jpeg\dct_cos_table.v line 1:70 mismatched character '\r' expecting '\n' | Sergey Smolov | Alexander Kamkin | 0.1 |
| 10215 | Verilog Translator | Bug | New | Normal | ERROR: Starting points limit has been exhausted: 2255 | Sergey Smolov | Alexander Kamkin | 0.1 |
| 10131 | Verilog Translator | Bug | Closed | Normal | ru.ispras.verilog.parser.VerilogIwlsTestCase.runTest_iscas_s9234_1: java.lang.OutOfMemoryError: Java heap space | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9993 | Verilog Translator | Bug | New | High | if two modules are passed to the tool and one includes another, the tool hangs | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9902 | Verilog Translator | Bug | New | High | java.lang.IllegalArgumentException: Descriptor for '<var name>' has not been found | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9803 | Verilog Translator | Bug | Closed | Normal | ru.ispras.verilog.parser.sample.MulFifoTestCase: NullPointerException at ru.ispras.verilog.parser.elaborator.VerilogElaborator$1.getNode(VerilogElaborator.java:932) | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9802 | Verilog Translator | Bug | Closed | Normal | ru.ispras.verilog.parser.sample.FuncTestCase: NullPointerException at ru.ispras.verilog.parser.elaborator.VerilogElaborator.createVariableAndBinding(VerilogElaborator.java:512) | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9798 | Verilog Translator | Bug | Closed | High | ru.ispras.verilog.parser.sample.Bug9798TestCase: incorrect BVEXTRACT params for bit vector variable with offset | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9775 | Verilog Translator | Bug | Closed | Normal | ru.ispras.verilog.parser.VerilogIeeeTestCase.runTest_10_04_04_1: Conversion = "" | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9773 | Verilog Translator | Bug | Rejected | Normal | ru.ispras.verilog.parser.VerilogIeeeTestCase.runTest_10_04_03_1: ru.ispras.fortress.expression.NodeOperation cannot be cast to ru.ispras.fortress.expression.NodeValue | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9594 | Verilog Translator | Bug | Closed | Normal | extra 'BVEXTRACT' operation in right hand side expression in 'assign' block's statement | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9296 | Verilog Translator | Bug | Closed | High | vcegar-tests/cache_coherence/two_processor_bin_2.v:46: illegal types of "then" and "else" expressions : unsigned word[1] and boolean | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9282 | Verilog Translator | Bug | Closed | High | ru.ispras.verilog.parser.sample.DataMemTestCase: DEBUG: Reduce: (BVEXTRACT 0 7 mem_access_addr) | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9276 | Verilog Translator | Bug | Rejected | Normal | no errors returned for bug-with-macro-containing module | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9250 | Verilog Translator | Bug | Closed | High | ru.ispras.verilog.parser.sample.IfStageTestCase: src/test/verilog/rest-tests/mips16/IF_stage.v line 31:9 missing KW_BEGIN at 'pc' | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9239 | Verilog Translator | Bug | Closed | High | ru.ispras.verilog.parser.sample.Mips16CoreTopTestCase: java.lang.IllegalArgumentException | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9224 | Verilog Translator | Bug | Closed | High | ru.ispras.verilog.parser.VerilogTexas97TestCase.runTest_PCI_BUS_Verilog_MV_files_PCInorm: ERROR: Function declaration '$random' has not been found | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9222 | Verilog Translator | Bug | Closed | High | ru.ispras.verilog.parser.VerilogVisVerilog2SmvTestCase.runTest_Sampleq_twoFifo1: java.lang.IllegalStateException: Parameter is not a value: LOGLENGTH | Sergey Smolov | Alexander Kamkin | 0.1 |

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| 9215 | Verilog Translator | Bug | Rejected | High | ru.ispras.verilog.parser.VerilogTexas97TestCase.runTest_PPC60X_bus_src_mem: Module 'AddrStatus' cannot be found | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9214 | Verilog Translator | Bug | Rejected | High | ru.ispras.verilog.parser.VerilogTexas97TestCase.runTest_PPC60X_bus_src_cpu: Module 'AddressTenure' cannot be found | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9213 | Verilog Translator | Bug | Rejected | High | ru.ispras.verilog.parser.VerilogTexas97TestCase.runTest_PPC60X_bus_src_arbiter: Module 'ArbiterStatus' cannot be found | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9212 | Verilog Translator | Bug | Closed | High | ru.ispras.verilog.parser.VerilogVisVerilog2SmvTestCase.runTest_Vlunc_vlunc: Module 'transform' cannot be found | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9211 | Verilog Translator | Bug | Closed | High | java.lang.IllegalArgumentException at ru.ispras.verilog.parser.model.VerilogModule.addDeclaration(VerilogModule.java:193) | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9210 | Verilog Translator | Bug | Closed | High | java.lang.IllegalArgumentException at ru.ispras.fortress.expression.Nodes.bvextract(Nodes.java:322) | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9202 | Verilog Translator | Bug | Closed | High | ru.ispras.verilog.parser.sample.PjIcuIcctl1TestCase: java.lang.ArrayIndexOutOfBoundsException: 3 | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9190 | Verilog Translator | Bug | Closed | High | ru.ispras.verilog.parser.sample.DescriptorBuffersTestCase: incorrect calculation for string parameter values | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9182 | Verilog Translator | Bug | Closed | High | ru.ispras.verilog.parser.sample.MulFifoTestCase: java.lang.IllegalStateException: Parameter is not a value: i | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9174 | Verilog Translator | Bug | Closed | High | NullPointerException via VerilogLiteral construction | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9173 | Verilog Translator | Bug | Closed | High | Incorrect DataType: BIT_VECTOR(1) instead of BIT_VECTOR(40) | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9165 | Verilog Translator | Bug | Closed | High | Incorrect parameter value calculation at hierarchical Verilog description | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9160 | Verilog Translator | Bug | Closed | High | ru.ispras.verilog.parser.sample.Mips16CoreTopTestCase: Module 'mips_16_core_top' cannot be found | Sergey Smolov | Alexander Kamkin | 0.1 |
| 9055 | Verilog Translator | Bug | Closed | High | Texas97IFetchVerilogPrinterTestCase: java.lang.IndexOutOfBoundsException: 4294967283 is out of bounds. | Sergey Smolov | Alexander Kamkin | 0.1 |
| 8990 | Verilog Translator | Bug | Closed | High | vcegar-benchmarks/pi_bus/main_1.v: incorrect translation of nested "if" conditions | Sergey Smolov | Alexander Kamkin | 0.1 |
| 8957 | Verilog Translator | Bug | Closed | High | wrong datatype for arrays | Sergey Smolov | Alexander Kamkin | 0.1 |
| 8865 | Verilog Translator | Bug | Closed | Normal | VerilogIeeeTestCase.runTest_19_11_00_1: java.lang.IllegalArgumentException: Declaration=DECLARATION(), parent=MODULE(m2) | Sergey Smolov | Alexander Kamkin | 0.1 |
| 8864 | Verilog Translator | Bug | Closed | Normal | VerilogIeeeTestCase.runTest_17_10_02_1_i: java.lang.IllegalArgumentException | Sergey Smolov | Alexander Kamkin | 0.1 |
| 8863 | Verilog Translator | Bug | Closed | Normal | VerilogIeeeTestCase.runTest_17_02_04_4_1: java.lang.IllegalArgumentException | Sergey Smolov | Alexander Kamkin | 0.1 |

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| 8862 | Verilog Translator | Bug | Closed | Normal | VerilogIeeeTestCase.runTest_12_08_02_1: java.lang.IllegalArgumentException | Sergey Smolov | Alexander Kamkin | 0.1 |
| 8861 | Verilog Translator | Bug | Closed | Normal | VerilogIeeeTestCase.runTest_12_04_03_1: java.lang.IllegalStateException: BigInteger data is not convertible to Boolean. | Sergey Smolov | Alexander Kamkin | 0.1 |
| 8860 | Verilog Translator | Bug | Closed | Normal | VerilogIeeeTestCase.runTest_12_04_02_4: java.lang.NullPointerException | Sergey Smolov | Alexander Kamkin | 0.1 |
| 8859 | Verilog Translator | Bug | Closed | Normal | VerilogIeeeTestCase.runTest_12_04_02_3: java.lang.NullPointerException | Sergey Smolov | Alexander Kamkin | 0.1 |
| 8858 | Verilog Translator | Bug | Closed | Normal | VerilogIeeeTestCase.runTest_12_04_01_2: java.lang.IllegalStateException: Parameter is not a value: (BVZEROEXT 2147483646 i) | Sergey Smolov | Alexander Kamkin | 0.1 |
| 8857 | Verilog Translator | Bug | Closed | Normal | VerilogIeeeTestCase.runTest_12_02_02_2_1: java.lang.NullPointerException | Sergey Smolov | Alexander Kamkin | 0.1 |
| 8856 | Verilog Translator | Bug | Closed | Normal | VerilogIeeeTestCase.runTest_10_04_05_1: java.lang.IllegalArgumentException | Sergey Smolov | Alexander Kamkin | 0.1 |
| 8855 | Verilog Translator | Bug | Closed | Normal | VerilogIeeeTestCase.runTest_10_03_00_5: java.lang.IllegalArgumentException | Sergey Smolov | Alexander Kamkin | 0.1 |
| 8854 | Verilog Translator | Bug | Closed | Normal | VerilogIeeeTestCase.runTest_05_02_02_2: java.lang.NullPointerException | Sergey Smolov | Alexander Kamkin | 0.1 |
| 8853 | Verilog Translator | Bug | Closed | Normal | VerilogIeeeTestCase.runTest_05_02_01_2: java.lang.IllegalArgumentException | Sergey Smolov | Alexander Kamkin | 0.1 |
| 8852 | Verilog Translator | Bug | Closed | Normal | VerilogIeeeTestCase.runTest_05_01_14_4: java.lang.NullPointerException | Sergey Smolov | Alexander Kamkin | 0.1 |
| 8851 | Verilog Translator | Bug | Closed | Normal | VerilogIeeeTestCase.runTest_05_01_14_3: java.lang.IllegalArgumentException: 0 must be > 0 | Sergey Smolov | Alexander Kamkin | 0.1 |
| 8850 | Verilog Translator | Bug | Closed | Normal | VerilogIeeeTestCase.runTest_05_01_14_1: java.lang.NullPointerException | Sergey Smolov | Alexander Kamkin | 0.1 |
| 8849 | Verilog Translator | Bug | Closed | Normal | VerilogIeeeTestCase.runTest_04_10_01_1 [floating point parameters]: java.lang.IllegalArgumentException | Sergey Smolov | Alexander Kamkin | 0.1 |
| 8848 | Verilog Translator | Bug | Closed | Normal | test_07_08_00_1.v: Module 'pullup' cannot be found | Sergey Smolov | Alexander Kamkin | 0.1 |
| 8847 | Verilog Translator | Bug | Closed | Normal | test_17_01_01_2_1.v:  Module 'pulldown' cannot be found | Sergey Smolov | Alexander Kamkin | 0.1 |
| 8846 | Verilog Translator | Bug | Closed | Normal | test_19_04_00_3.v:  Module 'real_last' cannot be found | Sergey Smolov | Alexander Kamkin | 0.1 |
| 8832 | Verilog Translator | Bug | Closed | Normal | verilog/opencores/mips16/IF_stage.v: java.lang.IllegalStateException: Parameter is not a value: (BVSUB 8 1) | Sergey Smolov | Alexander Kamkin | 0.1 |
| 8831 | Verilog Translator | Bug | Closed | Normal | vcegar-benchmarks/ipbdp/ipbdp_hier.v: java.lang.IllegalArgumentException: Bit vector sizes do not match: 4 != 32. | Sergey Smolov | Alexander Kamkin | 0.1 |

| # | Project | Tracker | Status | Priority | Subject | Author | Assignee | Target version |
|---|---|---|---|---|---|---|---|---|
| 8779 | Verilog Translator | Bug | Closed | Normal | mips16/data_mem.v: wrong type for define-containing declaration of 'ram_addr' wire | Sergey Smolov | Alexander Kamkin | 0.1 |
| 8738 | Verilog Translator | Bug | Closed | Normal | DataMemTestCase falls with error | Sergey Smolov | Alexander Kamkin | 0.1 |
| 6363 | Verilog Translator | Bug | Closed | High | src/test/verilog/fifo0/mem_2p.v: AbstractMethodError | Sergey Smolov | Alexander Kamkin | 0.1 |
| 6355 | Verilog Translator | Bug | Closed | High | src/test/verilog/fifo/fifo_testbench.v: NullPointerException | Sergey Smolov | Alexander Kamkin | 0.1 |
| 5567 | Verilog Translator | Bug | Closed | High | VerilogStaticChecker.ExpressionVisitor is not abstract and does not override abstract method getOperandOrder() in ExprTreeVisitor | Sergey Smolov | Alexander Kamkin | 0.1 |
| 5492 | Verilog Translator | Bug | Closed | Normal | retrascope + sapic.v = java.lang.IllegalStateException: Operand is not a constant integer value: 00000000000000000000000000000011 | Sergey Smolov | Alexander Kamkin | 0.1 |
| 10245 | Verilog Translator | Bug | Closed | Normal | ru.ispras.verilog.parser.VerilogQuipTestSuite#runTest_pci_wbw_wbr_fifos: ERROR: [Internal] null | Sergey Smolov | Alexey Danilov | 0.1 |
| 10237 | Verilog Translator | Bug | Closed | High | ru.ispras.verilog.parser.VerilogTexas97TestSuite#runTest_Pi_Bus_single_master_main2: ERROR: Cycle inclusion at: '...bus.v' | Sergey Smolov | Alexey Danilov | 0.1 |
| 10216 | Verilog Translator | Bug | Closed | High | ru.ispras.verilog.parser.VerilogQuipTestSuite#runTest_nut_001: java.lang.NullPointerException | Sergey Smolov | Alexey Danilov | 0.1 |
| 10173 | Verilog Translator | Bug | Closed | High | javadoc: DefineStructure.java:37: warning: no @return | Sergey Smolov | Alexey Danilov | 0.1 |
| 10141 | Verilog Translator | Bug | Closed | Normal | check port redeclarations | Sergey Smolov | Alexey Danilov | 0.1 |
| 9962 | Verilog Translator | Bug | Closed | High | ru.ispras.verilog.parser.sample.Mips16CoreTopTestCase: java.lang.IllegalArgumentException | Sergey Smolov | Alexey Danilov | 0.1 |
| 9936 | Verilog Translator | Bug | Closed | High | tabs in "`define" directive cause java.lang.NumberFormatException | Sergey Smolov | Alexey Danilov | 0.1 |
| 9915 | Verilog Translator | Bug | Closed | Urgent | "Cycle inclusion has been detected in fine <filename>" error is reported for Verilog modules that use the same another file | Sergey Smolov | Alexey Danilov | 0.1 |

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