

Issues

#	Project	Tracker	Status	Priority	Subject	Author	Assignee	Target version
2494	CTESK	Bug	New	Normal	warning at build log	Sergey Smolov	Alexey Demakov	
3528	Local Support Project	Bug	Closed	Normal	Не отображается полный адрес svn-репозитория	Sergey Smolov	Alexey Demakov	
3565	Local Support Project	Bug	Closed	Normal	Перестали приходить уведомления на почту об изменениях в проектах	Sergey Smolov	Alexey Demakov	
3590	C++TESK Testing ToolKit	Bug	Closed	Normal	C++TesK installation fails on OpenSUSE 12.2 x64	Sergey Smolov	Sergey Smolov	1.0
3605	Retrascope	Bug	Rejected	Normal	[vhdl][parser][cfg] Zаміа не обрабатывает пакеты функций	Sergey Smolov	Sergey Smolov	0.1
3622	Retrascope	Bug	Closed	Normal	DFGElementaryCyclesTest & DFGClusterStatisticsTest - java.lang.OutOfMemoryError: Java heap space	Sergey Smolov	Sergey Smolov	
3717	C++TESK Development Environment	Bug	Closed	Normal	Переименовать com.unitesk.cpptestk.ide.prototype.presentations в com.unitesk.cpptestk.ide.prototype.ir	Sergey Smolov	Sergey Smolov	
3757	C++TESK Development Environment	Bug	Closed	Normal	Добавить jar-ник SWT в проект com.unitesk.cpptestk.ide.mapper	Sergey Smolov	Sergey Smolov	
3805	C++TESK Testing ToolKit	Bug	Closed	Normal	Ошибка в QuickReference	Sergey Smolov	Sergey Smolov	
3980	Retrascope	Bug	Closed	Normal	ru.ispras.retrascope.cfg.lib.examples.FIFOExample.java compilation error	Sergey Smolov	Sergey Smolov	
4004	C++TESK Testing ToolKit	Bug	Closed	Normal	Из build'a пропал скрипт install-eclipse-plugin.sh	Sergey Smolov	Sergey Smolov	1.0
4005	C++TESK Testing ToolKit	Bug	Rejected	Normal	удалить пустой README	Sergey Smolov	asd ert	1.0
4221	Fortress	Bug	Closed	Normal	performConstant: public -> private	Sergey Smolov	Sergey Smolov	0.2
4357	Retrascope	Bug	Closed	Normal	[cfg][transformer][cгаа] Внести исправления в методы извлечения clock-like variables	Sergey Smolov	Sergey Smolov	0.1
4358	Retrascope	Bug	Closed	Normal	Внести исправления в представление CGA и методы их извлечения	Sergey Smolov	Sergey Smolov	
4464	MicroTESK	Bug	Closed	Normal	[project] ошибки сборки проекта в Eclipse	Sergey Smolov	Andrei Tatarnikov	
4797	Fortress	Bug	Closed	Normal	[solver] NullPointerException when solver is not found	Sergey Smolov	Andrei Tatarnikov	0.3
4813	Fortress	Bug	Closed	High	[solver][constraint] Невозможно создавать тривиальные ограничения	Sergey Smolov	Andrei Tatarnikov	0.3
4836	Retrascope	Bug	Closed	Normal	[cfg][transformer][cгаа] java heap space error at control.vhdl/mlite2sram.vhdl	Sergey Smolov	Sergey Smolov	0.1
4926	Retrascope	Bug	Closed	Normal	[cfg][model] Путаница с наследниками CfgNode	Sergey Smolov	Sergey Smolov	0.1
4928	Retrascope	Bug	Rejected	Normal	[cfg] Range может состоять из нескольких участков	Sergey Smolov	Sergey Smolov	0.1
4991	Retrascope IDE	Bug	Closed	Normal	Не передается путь к HDL-описанию	Sergey Smolov	Alexander Kamkin	
5003	Retrascope	Bug	Rejected	Normal	[util] XmlUtilTest.java: java.lang.RuntimeException: An error occurred while trying to resolve a constraint.	Sergey Smolov	Igor Melnichenko	0.1

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5510	Retrascope	Bug	Closed	High	[efsm][generator][test] RandomFateSequenceliterator compilation error	Sergey Smolov	Igor Melnichenko	0.1
5524	Retrascope	Bug	Closed	High	[engine][xml] wrong package for TestXmlPrinter	Sergey Smolov	Igor Melnichenko	0.1
5525	Retrascope	Bug	Closed	High	[engine][xml] wrong package for TestXmlPrinterTestCase	Sergey Smolov	Igor Melnichenko	0.1
5528	Retrascope	Bug	Closed	High	[engine][testbench] java.nio.file.FileAlreadyExistsException: decider_parser.vhd	Sergey Smolov	Igor Melnichenko	0.1
5536	Retrascope	Bug	Closed	Normal	[efsm][generator][test] E fsmTestGeneratorVhdlTestCase -> java.lang.RuntimeException: Unexpected simulation result	Sergey Smolov	Igor Melnichenko	0.1
5538	Retrascope	Bug	Closed	Normal	[efsm][generator][test] E fsmFateTestGeneratorVhdlTestCase -> java.lang.RuntimeException: Unexpected simulation result.	Sergey Smolov	Igor Melnichenko	0.1
5540	Retrascope	Bug	Closed	Normal	[javadoc] E fsmSimulator.java:119: warning - @param argument "efsm" is not a parameter name.	Sergey Smolov	Igor Melnichenko	0.1
5547	Retrascope IDE	Bug	New	Normal	save Retrascope result not to ECLIPSE_HOME folder	Sergey Smolov		0.1
5567	Verilog Translator	Bug	Closed	High	VerilogStaticChecker.ExpressionVisitor is not abstract and does not override abstract method getOperandOrder() in ExprTreeVisitor	Sergey Smolov	Alexander Kamkin	0.1
5572	Retrascope	Bug	Closed	Normal	[efsm][simulator] b10: Failed to resolve the assignment constraint	Sergey Smolov	Igor Melnichenko	0.1
5608	Retrascope	Bug	Closed	High	[efsm][generator][test][fate] FATE generator hangs at b03 description from ITC'99	Sergey Smolov	Igor Melnichenko	0.1
5648	Retrascope	Bug	Rejected	High	E fsmSimulator.executeAssignment -> Unsupported data type of ranged variable: (MAP LOGIC_INTEGER LOGIC_INTEGER)	Sergey Smolov	Igor Melnichenko	0.2
5680	Retrascope	Bug	Closed	Urgent	[efsm][generator][test][fate] DirectedFateGenerator.generateSequence -> NullPointerException	Sergey Smolov	Igor Melnichenko	0.1
5684	Retrascope	Bug	Rejected	Low	computeExpression -> LOGIC_BOOLEAN vs (MAP LOGIC_INTEGER LOGIC_BOOLEAN)	Sergey Smolov	Igor Melnichenko	0.2
5692	Retrascope	Bug	Rejected	Normal	FATE/FATE+ hangs on b03 with Java 1.8	Sergey Smolov	Igor Melnichenko	
5709	Retrascope	Bug	Closed	Normal	TestMinimiser.java:43: warning - @param argument "test" is not a parameter name.	Sergey Smolov	Igor Melnichenko	0.1
5715	Retrascope	Bug	Closed	High	E fsmTestGenerator.java:138: error: method put in interface Map<K,V> cannot be applied to given types -> traversedPaths.put(efsm, new HashSet<>());	Sergey Smolov	Igor Melnichenko	0.1
5719	Retrascope	Bug	Closed	Urgent	EFSM Test Generator hangs on b11	Sergey Smolov	Igor Melnichenko	0.1
5736	Retrascope	Bug	Closed	Normal	E fsmSimulator.substituteVariables(E fsmSimulator.java:736) -> NullPointerException	Sergey Smolov	Igor Melnichenko	0.1
5778	Retrascope	Bug	Closed	Normal	ru.ispras.retrascope.engine.testbench.TestVhdlTestbenchPrinterTestCase -> java.util.NoSuchElementException	Sergey Smolov	Igor Melnichenko	0.1
5827	Retrascope	Bug	Closed	Normal	TestVhdlTestbenchPrinterDummyTestCase -> NoSuchFileException	Sergey Smolov	Igor Melnichenko	0.1
5828	Retrascope	Bug	Closed	Normal	TestVhdlTestbenchPrinterVhdlTestCase -> IllegalArgumentException: Unexpected event value: true	Sergey Smolov	Igor Melnichenko	0.1
5831	Retrascope	Bug	Closed	Normal	E fsmSimulator.java -> Tag @see: can't find getResetGuardedAction() in ru.ispras.retrascope.model.efsm.E fsm	Sergey Smolov	Igor Melnichenko	0.1
5836	Local Support Project	Bug	Resolved	High	не собирается проект на сервере Jenkins	Sergey Smolov	Sergey Smolov	
5871	Retrascope	Bug	Closed	Normal	ru.ispras.retrascope.test.printer.testbench -> ru.ispras.retrascope.engine.test.printer.testbench	Sergey Smolov	Igor Melnichenko	0.1

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5873	Retrascope	Bug	Closed	High	missing transitions in b04 EFSM	Sergey Smolov	Sergey Smolov	0.1
5966	MicroTESK	Bug	Closed	Normal	mark shell scripts as executable in the distribution tar.gz archive	Sergey Smolov	Sergey Smolov	2.5
6106	MicroTESK	Bug	Closed	Normal	zero opcodes for instructions in Tarmac log	Sergey Smolov	Andrei Tatarnikov	2.2
6241	MicroTESK	Bug	Closed	Normal	Generated assembler files contain tab-only lines	Sergey Smolov	Andrei Tatarnikov	2.2
6263	Retrascope	Bug	Closed	High	Crash when test generation engine elaborates EFSMs from alu.vhd: java.lang.IllegalArgumentException	Sergey Smolov	Sergey Smolov	0.2
6279	Retrascope	Bug	Closed	Normal	TestXmlPrinterTestCase: IllegalArgumentException: Output file name isn't specified	Sergey Smolov	Igor Melnichenko	0.1
6280	Retrascope	Bug	Closed	Normal	TestVhdlTestbenchPrinterVhdlTestCase: The exception has occurred while printing test pattern file	Sergey Smolov	Igor Melnichenko	0.1
6281	Retrascope	Bug	Closed	Normal	E fsmTestGeneratorVhdlTestCase: E fsm.UNINITIALISED_STATE isn't supported yet	Sergey Smolov	Sergey Smolov	0.1
6293	Retrascope	Bug	Closed	Normal	XmlTestParserTestCase: NoSuchMethodException	Sergey Smolov	Igor Melnichenko	0.1
6335	Retrascope	Bug	Closed	Normal	fifo.v: non-constant number of extracted EFSMs' transitions	Sergey Smolov	Sergey Smolov	0.1
6352	Fortress	Bug	Closed	High	Transformer.standardize returns 'false' on (AND (EQ a 00) (NOT(EQ a b 00)))	Sergey Smolov	Artem Kotsynyak	0.4
6353	Retrascope	Bug	Closed	Normal	Case children of one Switch node can have equal NodeValue	Sergey Smolov	Sergey Smolov	0.1
6355	Verilog Translator	Bug	Closed	High	src/test/verilog/fifo/fifo_testbench.v: NullPointerException	Sergey Smolov	Alexander Kamkin	0.1
6362	Retrascope	Bug	Rejected	Normal	src/test/verilog/adder/adder4_testbench.v: wrong CFG model	Sergey Smolov	Mikhail Chupilko	0.1
6363	Verilog Translator	Bug	Closed	High	src/test/verilog/fifo0/mem_2p.v: AbstractMethodError	Sergey Smolov	Alexander Kamkin	0.1
6365	Retrascope	Bug	Closed	Normal	src/test/vhdl/example/example.vhd: IllegalArgumentException	Sergey Smolov	Mikhail Lebedev	0.1
6366	Retrascope	Bug	Rejected	Normal	src/test/vhdl/example/test.vhd: E fsm.UNINITIALISED_STATE isn't supported yet	Sergey Smolov	Igor Melnichenko	0.2
6375	Retrascope	Bug	Closed	Normal	missing javadoc	Sergey Smolov	Igor Melnichenko	0.1
6394	Local Support Project	Bug	New	Normal	Проект HDL Retrascope: на 17-дюймовом мониторе не масштабируется таблица Задачи	Sergey Smolov	Alexey Demakov	
6413	Retrascope	Bug	Closed	Normal	b03.vhd: different EFSM extraction stats	Sergey Smolov	Sergey Smolov	0.1
6424	Retrascope	Bug	Closed	Normal	b05.vhd: line 64: at token "d32_-10": syntax error	Sergey Smolov	Mikhail Lebedev	0.1
6425	Retrascope	Bug	Closed	Normal	b12.vhd: XmvExprPrinter.getConstant(XmvExprPrinter.java:330) -> NullPointerException	Sergey Smolov	Mikhail Lebedev	0.1
6426	Retrascope	Bug	Closed	Normal	example.vhd: HlddXmvVisitor.onProcessEnd(HlddXmvVisitor.java:381) -> NullPointerException	Sergey Smolov	Mikhail Lebedev	0.1
6430	Retrascope	Bug	Closed	Normal	b14.vhd: StackOverflowError	Sergey Smolov	Sergey Smolov	0.2
6443	Retrascope	Bug	Closed	Normal	print error message when "--toplevel" value is wrong	Sergey Smolov	Sergey Smolov	0.1
6504	Retrascope	Bug	Closed	Normal	fifo/fifo.v: nuSMV model checker returns ERROR	Sergey Smolov	Mikhail Lebedev	0.1
6510	Retrascope	Bug	Closed	Normal	fix javadoc	Sergey Smolov	Mikhail Lebedev	0.1
6730	Retrascope	Bug	Closed	Normal	fix javadoc	Sergey Smolov	Mikhail Lebedev	0.1

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6892	Retrascope	Bug	Closed	Normal	support for non-zero starting bitvectors	Sergey Smolov	Sergey Smolov	0.2
6959	Retrascope IDE	Bug	Closed	High	java.lang.NullPointerException at startup	Sergey Smolov	Sergey Smolov	0.1
6984	Retrascope IDE	Bug	Closed	Normal	java.io.IOException: Unable to resolve plug-in "platform:/plugin/retrascope-ide/icons/retrascope.gif".	Sergey Smolov	Sergey Smolov	0.1
7097	Retrascope	Bug	Closed	Normal	32-bit constants should be casted to appropriate values	Sergey Smolov	Sergey Smolov	0.2
7098	Verilog Translator	Bug	Closed	Normal	src/test/verilog/mips16/data_mem.v: 'mem_access_addr' has null declaration	Sergey Smolov	Sergey Smolov	0.1
7145	Retrascope	Bug	Closed	Normal	cfg-rnd-testgen: take variable invariants into account	Sergey Smolov	Sergey Smolov	0.2
7166	Retrascope	Bug	Closed	Normal	cfg-rnd-testgen: OutOfMemoryError at b10 (1.000.000 ticks)	Sergey Smolov	Sergey Smolov	0.2
7423	Retrascope	Bug	Rejected	High	rnd_fsm.vhd: empty tst file	Sergey Smolov	Igor Melnichenko	0.2
7474	Verilog Translator	Bug	Closed	Normal	missing empty branches for 'if' statements	Sergey Smolov	Sergey Smolov	0.1
7555	Fortress	Bug	Closed	Normal	unable to create constraint-related junit tests including unused variables	Sergey Smolov	Artem Kotsynyak	0.4
7557	Fortress	Bug	Closed	High	ConstCastTestCase: java.lang.AssertionError: Calculator failed to substitute result	Sergey Smolov	Artem Kotsynyak	0.4
7576	Retrascope	Bug	Closed	Normal	mips16/hazard_detection_unit.v: java.lang.IllegalArgumentException: Constraint contains errors	Sergey Smolov	Sergey Smolov	0.2
7593	Retrascope	Bug	Closed	Normal	mips16/data_mem.v: java.lang.IllegalArgumentException	Sergey Smolov	Sergey Smolov	0.2
7594	Retrascope	Bug	Rejected	Normal	ModelSim shows error when TST file contains multiple comments	Sergey Smolov	Sergey Smolov	0.2
7720	Retrascope	Bug	Closed	Normal	mips16/data_mem.v: The expression to be computed (ram) contains unevaluated variables: [ram]	Sergey Smolov	Sergey Smolov	0.2
7730	MicroTESK	Bug	Closed	High	[tarmac-logger] missing "<cpu>" tag	Sergey Smolov	Andrei Tatarnikov	2.4
7753	Retrascope	Bug	Closed	Normal	example.vhd: cannot generate SMV-based test	Sergey Smolov	Sergey Smolov	0.2
7883	Retrascope	Bug	Closed	Normal	fifo_testbench.v: java.lang.NullPointerException	Sergey Smolov	Sergey Smolov	0.2
8237	Retrascope	Bug	Closed	Normal	CFG random test generator works too slow on b19	Sergey Smolov	Sergey Smolov	0.2
8242	Trace Matcher	Bug	Closed	Normal	print hexadecimal values to the output file in the same form as they were at input files	Sergey Smolov	Sergey Smolov	0.1
8244	Retrascope	Bug	Closed	Normal	CGAA-to-EFSM engine falls on b05 test	Sergey Smolov	Sergey Smolov	0.2
8245	Retrascope	Bug	Closed	Normal	cfg-rnd-testgen: IllegalArgumentException at minimips\pps_pf.v	Sergey Smolov	Sergey Smolov	0.2
8283	Retrascope	Bug	Closed	Normal	"X <= (others => '0')" should be translated properly when X is bit vector	Sergey Smolov	Sergey Smolov	0.2
8285	Retrascope	Bug	Closed	Normal	0% coverage of EFSM transitions for b01 example	Sergey Smolov	Sergey Smolov	0.2
8289	Retrascope	Bug	Closed	Normal	ITC99 b02: no resetting transition has been found	Sergey Smolov	Sergey Smolov	0.2
8573	Fortress	Bug	Closed	Normal	missing javadoc	Sergey Smolov	Andrei Tatarnikov	0.4
8681	Retrascope	Bug	Closed	Normal	EngineRegistry fails to create toolchain when HashSet\HashMap are used	Sergey Smolov	Alexander Kamkin	1.0
8738	Verilog Translator	Bug	Closed	Normal	DataMemTestCase falls with error	Sergey Smolov	Alexander Kamkin	0.1

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8779	Verilog Translator	Bug	Closed	Normal	mips16/data_mem.v: wrong type for define-containing declaration of 'ram_addr' wire	Sergey Smolov	Alexander Kamkin	0.1
8786	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.sample.FifoTestbenchTestCase fails	Sergey Smolov	Sergey Smolov	0.1
8831	Verilog Translator	Bug	Closed	Normal	vcegar-benchmarks/ipbdp/ipbdp_hier.v: java.lang.IllegalArgumentException: Bit vector sizes do not match: 4 != 32.	Sergey Smolov	Alexander Kamkin	0.1
8832	Verilog Translator	Bug	Closed	Normal	verilog/opencores/mips16/IF_stage.v: java.lang.IllegalStateException: Parameter is not a value: (BVSUB 8 1)	Sergey Smolov	Alexander Kamkin	0.1
8846	Verilog Translator	Bug	Closed	Normal	test_19_04_00_3.v: Module 'real_last' cannot be found	Sergey Smolov	Alexander Kamkin	0.1
8847	Verilog Translator	Bug	Closed	Normal	test_17_01_01_2_1.v: Module 'pulldown' cannot be found	Sergey Smolov	Alexander Kamkin	0.1
8848	Verilog Translator	Bug	Closed	Normal	test_07_08_00_1.v: Module 'pullup' cannot be found	Sergey Smolov	Alexander Kamkin	0.1
8849	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_04_10_01_1 [floating point parameters]: java.lang.IllegalArgumentException	Sergey Smolov	Alexander Kamkin	0.1
8850	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_05_01_14_1: java.lang.NullPointerException	Sergey Smolov	Alexander Kamkin	0.1
8851	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_05_01_14_3: java.lang.IllegalArgumentException: 0 must be > 0	Sergey Smolov	Alexander Kamkin	0.1
8852	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_05_01_14_4: java.lang.NullPointerException	Sergey Smolov	Alexander Kamkin	0.1
8853	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_05_02_01_2: java.lang.IllegalArgumentException	Sergey Smolov	Alexander Kamkin	0.1
8854	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_05_02_02_2: java.lang.NullPointerException	Sergey Smolov	Alexander Kamkin	0.1
8855	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_10_03_00_5: java.lang.IllegalArgumentException	Sergey Smolov	Alexander Kamkin	0.1
8856	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_10_04_05_1: java.lang.IllegalArgumentException	Sergey Smolov	Alexander Kamkin	0.1
8857	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_12_02_02_2_1: java.lang.NullPointerException	Sergey Smolov	Alexander Kamkin	0.1
8858	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_12_04_01_2: java.lang.IllegalStateException: Parameter is not a value: (BVZEROEXT 2147483646 i)	Sergey Smolov	Alexander Kamkin	0.1
8859	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_12_04_02_3: java.lang.NullPointerException	Sergey Smolov	Alexander Kamkin	0.1
8860	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_12_04_02_4: java.lang.NullPointerException	Sergey Smolov	Alexander Kamkin	0.1

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8861	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_12_04_03_1: java.lang.IllegalStateException: BigInteger data is not convertible to Boolean.	Sergey Smolov	Alexander Kamkin	0.1
8862	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_12_08_02_1: java.lang.IllegalArgumentException	Sergey Smolov	Alexander Kamkin	0.1
8863	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_17_02_04_4_1: java.lang.IllegalArgumentException	Sergey Smolov	Alexander Kamkin	0.1
8864	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_17_10_02_1_i: java.lang.IllegalArgumentException	Sergey Smolov	Alexander Kamkin	0.1
8865	Verilog Translator	Bug	Closed	Normal	VerilogIeeeTestCase.runTest_19_11_00_1: java.lang.IllegalArgumentException: Declaration=DECLARATION(), parent=MODULE(m2)	Sergey Smolov	Alexander Kamkin	0.1
8912	Retrascope	Bug	Closed	Normal	file ram.smv: line 332: variable is assigned more than once: m_ram.mem0	Sergey Smolov	Sergey Smolov	1.0
8957	Verilog Translator	Bug	Closed	High	wrong datatype for arrays	Sergey Smolov	Alexander Kamkin	0.1
8990	Verilog Translator	Bug	Closed	High	vcegar-benchmarks/pi_bus/main_1.v: incorrect translation of nested "if" conditions	Sergey Smolov	Alexander Kamkin	0.1
8991	Retrascope	Bug	Closed	Normal	CfgSwitchSequenceBackend: do not collapse "if" statements with incompatible conditions	Sergey Smolov	Sergey Smolov	1.0
9010	Retrascope Test Suite	Bug	Closed	Normal	Texas97CacheCoherenceVerilogPrinterTestCase: java.lang.IllegalArgumentException	Sergey Smolov	Sergey Smolov	
9011	Retrascope Test Suite	Bug	Closed	Normal	Texas97IFetchVerilogPrinterTestCase: java.lang.IndexOutOfBoundsException: 4294967283 is out of bounds.	Sergey Smolov	Sergey Smolov	
9012	Retrascope Test Suite	Bug	Closed	Normal	VisBufferAllocVerilogPrinterTestCase: java.lang.IllegalArgumentException	Sergey Smolov		
9055	Verilog Translator	Bug	Closed	High	Texas97IFetchVerilogPrinterTestCase: java.lang.IndexOutOfBoundsException: 4294967283 is out of bounds.	Sergey Smolov	Alexander Kamkin	0.1
9063	MicroTESK	Bug	Closed	Normal	microtesk/src/main/java/core/ru/ispras/microtesk/utills/PropertyMap.java uses unchecked or unsafe operations	Sergey Smolov	Alexander Kamkin	2.5
9066	Retrascope	Bug	Closed	Normal	ru.ispras.retrascope.engine.hidd.printer.smv.Texas97HiddSmvPrinterTestCase.runTest: java.lang.NullPointerException	Sergey Smolov	Sergey Smolov	1.0
9071	Retrascope Test Suite	Bug	Open	Normal	ru.ispras.retrascope.engine.hidd.printer.smv.Texas97HiddSmvPrinterTestCase.runTest: java.lang.IllegalArgumentException: Unknown operation 'FUNCTION'	Sergey Smolov	Mikhail Lebedev	
9075	Retrascope	Bug	Closed	Normal	java.lang.IllegalArgumentException: testNum 0 != 1 topModuleNum	Sergey Smolov	Sergey Smolov	1.0
9160	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.sample.Mips16CoreTopTestCase: Module 'mips_16_core_top' cannot be found	Sergey Smolov	Alexander Kamkin	0.1
9165	Verilog Translator	Bug	Closed	High	Incorrect parameter value calculation at hierarchical Verilog description	Sergey Smolov	Alexander Kamkin	0.1
9172	Retrascope Test Suite	Bug	Closed	Normal	Texas97ParsepackCfgGraphMITTestCase: ru.ispras.retrascope.basis.exception.RetrascopeException: Wrong range: 0 < 0 or 7 > 1.	Sergey Smolov	Sergey Smolov	
9173	Verilog Translator	Bug	Closed	High	Incorrect DataType: BIT_VECTOR(1) instead of BIT_VECTOR(40)	Sergey Smolov	Alexander Kamkin	0.1

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9174	Verilog Translator	Bug	Closed	High	NullPointerException via VerilogLiteral construction	Sergey Smolov	Alexander Kamkin	0.1
9175	Retrascope Test Suite	Bug	Closed	Normal	Texas97PdlxCfgGraphMITestCase: NullPointerException	Sergey Smolov	Sergey Smolov	
9176	Retrascope Test Suite	Bug	Closed	Normal	VcegarHlddSmvPrinterTestCase: java.lang.IllegalArgumentException: Unknown operation 'BVSDIV'	Sergey Smolov	Mikhail Lebedev	
9182	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.sample.MulFifoTestCase: java.lang.IllegalStateException: Parameter is not a value: i	Sergey Smolov	Alexander Kamkin	0.1
9184	Veritool	Bug	New	Normal	ERROR: Unable to read config file: /usr/lib/x86_64-linux-gnu/ivl/veritool.conf	Sergey Smolov		
9190	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.sample.DescriptorBuffersTestCase: incorrect calculation for string parameter values	Sergey Smolov	Alexander Kamkin	0.1
9202	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.sample.PjIcucctl1TestCase: java.lang.ArrayIndexOutOfBoundsException: 3	Sergey Smolov	Alexander Kamkin	0.1
9203	Retrascope Test Suite	Bug	Closed	Normal	ru.ispras.retrascope.basis.HlddAssertSmvTestbenchBenchmarkTest.runTest: java.lang.IllegalArgumentException: 'benchmarks' field is not initialized.	Sergey Smolov	Mikhail Lebedev	
9209	Verilog Translator	Bug	Closed	High	java.util.EmptyStackException at ru.ispras.verilog.parser.util.TokenSourceStack.getLastParentToken(TokenSourceStack.java:70)	Sergey Smolov	Sergey Smolov	0.1
9210	Verilog Translator	Bug	Closed	High	java.lang.IllegalArgumentException at ru.ispras.fortress.expression.Nodes.bvextract(Nodes.java:322)	Sergey Smolov	Alexander Kamkin	0.1
9211	Verilog Translator	Bug	Closed	High	java.lang.IllegalArgumentException at ru.ispras.verilog.parser.model.VerilogModule.addDeclaration(VerilogModule.java:193)	Sergey Smolov	Alexander Kamkin	0.1
9212	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.VerilogVisVerilog2SmvTestCase.runTest_Vlunc_vlunc: Module 'transform' cannot be found	Sergey Smolov	Alexander Kamkin	0.1
9213	Verilog Translator	Bug	Rejected	High	ru.ispras.verilog.parser.VerilogTexas97TestCase.runTest_PPC60X_bus_src_arbiter: Module 'ArbiterStatus' cannot be found	Sergey Smolov	Alexander Kamkin	0.1
9214	Verilog Translator	Bug	Rejected	High	ru.ispras.verilog.parser.VerilogTexas97TestCase.runTest_PPC60X_bus_src_cpu: Module 'AddressTenure' cannot be found	Sergey Smolov	Alexander Kamkin	0.1
9215	Verilog Translator	Bug	Rejected	High	ru.ispras.verilog.parser.VerilogTexas97TestCase.runTest_PPC60X_bus_src_mem: Module 'AddrStatus' cannot be found	Sergey Smolov	Alexander Kamkin	0.1
9222	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.VerilogVisVerilog2SmvTestCase.runTest_Sampleq_twoFifo1: java.lang.IllegalStateException: Parameter is not a value: LOGLENGTH	Sergey Smolov	Alexander Kamkin	0.1
9223	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.VerilogVcegarTestCase.runTest_pj_icu_icctl1: ERROR: Declaration of 'clk' has not been found	Sergey Smolov	Mikhail Lebedev	0.1
9224	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.VerilogTexas97TestCase.runTest_PCI_BUS_Verilog_MV_files_PCInorm: ERROR: Function declaration '\$random' has not been found	Sergey Smolov	Alexander Kamkin	0.1
9225	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.VerilogTexas97TestCase.runTest_MPEG_prefixcode: ERROR: ../texas97-tests/MPEG/prefixcode.v line 70:8 no viable alternative at input ';	Sergey Smolov	Mikhail Lebedev	0.1

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9226	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.VerilogVcegarTestCase.runTest_small_pipeline_pipeline_smv: /src/test/verilog/vcegar-tests/small/pipeline/pipeline_smv.v line 38:10 no viable alternative at input 'property'	Sergey Smolov	Mikhail Lebedev	0.1
9230	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.VerilogTexas97TestCase.runTest_PI_BUS_multi_master_bus: java.lang.IllegalArgumentException	Sergey Smolov	Sergey Smolov	0.1
9231	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.VerilogTexas97TestCase.runTest_PI_BUS_single_master_master2: java.lang.NullPointerException	Sergey Smolov	Sergey Smolov	0.1
9239	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.sample.Mips16CoreTopTestCase: java.lang.IllegalArgumentException	Sergey Smolov	Alexander Kamkin	0.1
9250	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.sample.IfStageTestCase: src/test/verilog/rest-tests/mips16/IF_stage.v line 31:9 missing KW_BEGIN at 'pc'	Sergey Smolov	Alexander Kamkin	0.1
9276	Verilog Translator	Bug	Rejected	Normal	no errors returned for bug-with-macro-containing module	Sergey Smolov	Alexander Kamkin	0.1
9282	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.sample.DataMemTestCase: DEBUG: Reduce: (BVEXTRACT 0 7 mem_access_addr)	Sergey Smolov	Alexander Kamkin	0.1
9288	QEMU4V	Bug	Closed	Immediate	/target/mips/translate.c:2617:9: error: 'else' without a previous 'if'	Sergey Smolov	Maxim Chudnov	0.2
9296	Verilog Translator	Bug	Closed	High	vcegar-tests/cache_coherence/two_processor_bin_2.v:46: illegal types of "then" and "else" expressions : unsigned word[1] and boolean	Sergey Smolov	Alexander Kamkin	0.1
9309	Retrascope Test Suite	Bug	Closed	Normal	ru.ispras.retrascope.engine.smv.testbench.sample.vcegar.VcegarPiBusAssertSmvTestbench TestCase:line 2 column 34: invalid declaration, builtin symbol select	Sergey Smolov	Sergey Smolov	
9333	QEMU4V	Bug	Closed	Normal	unexpected hex value in MIPS trace	Sergey Smolov	Sergey Smolov	0.2
9334	QEMU4V	Bug	Closed	Normal	timestamp reset at MIPS trace	Sergey Smolov	Sergey Smolov	0.2
9365	QEMU4V	Bug	Closed	Normal	missing insn binary images in MIPS trace	Sergey Smolov	Sergey Smolov	0.2
9374	MicroTESK for PowerPC	Bug	Closed	Normal	ru.ispras.microtesk.model.powerpc.autogen.BoundaryTestCase: Simulation failedThe CPR storage is not defined in the model.ru.ispras.microtesk.model.ConfigurationException: The CPR storage is not defined in the model.	Sergey Smolov	Alexander Protsenko	
9375	MicroTESK for PowerPC	Bug	Closed	Normal	ru.ispras.microtesk.model.powerpc.autogen.GroupTestCase: org.jruby.exceptions.RaiseException: (NoMethodError) undefined method `la' for #<GroupGenTemplate:0x6046f0da>	Sergey Smolov	Alexander Protsenko	
9376	MicroTESK for MIPS	Bug	New	Normal	Warning: Group MIPS64FpuOp contains two items add_fmt and mfc1 with the same opcode 01000100000000000000000000000000	Sergey Smolov	Alexander Kamkin	
9377	MicroTESK for MIPS	Bug	New	Normal	'Failed to construct decoder' warnings in project's build log	Sergey Smolov	Alexander Kamkin	
9386	MicroTESK for PowerPC	Bug	Closed	High	ru.ispras.microtesk.model.powerpc.InstructionALUTestCase: Assembler messages: ./microtesk-powerpc/build/test/instruction_alu/instruction_alu_0000.s:1: Error: junk at end of line, first unrecognized character is `/'	Sergey Smolov	Sergey Smolov	
9387	MicroTESK for PowerPC	Bug	Closed	Normal	ru.ispras.microtesk.model.powerpc.InstructionBPUTestCase: ./microtesk-powerpc/build/test/instruction_bpu/instruction_bpu_0000.s:47: Error: operand out of range (0x00000000000002774 is not between 0x0000000000000000 and 0x0000000000000001	Sergey Smolov	Alexander Protsenko	

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9436	MicroTESK	Bug	Closed	Normal	ru.ispras.microtesk.mmu.translator.GeneralTestCase: java.lang.IllegalArgumentException	Sergey Smolov	Alexander Kamkin	2.5
9437	MicroTESK	Bug	Closed	Normal	ru.ispras.microtesk.model.minimips.BufferPreparatorTestCase: QEMU4V crashes with general protection error on this test program	Sergey Smolov	Sergey Smolov	2.4
9463	Retrascope	Bug	Closed	Normal	check if junit test cases for CfgCgaaTransformer return same results on different machines\platforms	Sergey Smolov	Sergey Smolov	1.0
9475	Retrascope RISC-V Benchmark	Bug	Closed	Normal	Picorv32Hx8kdemoVerilogPrinterTestCase: ERROR: line 1:0 no viable alternative at input '('	Sergey Smolov	Alexander Kamkin	
9477	Retrascope RISC-V Benchmark	Bug	New	Normal	an "import "DPI-C" function" construction causes Verilog Translator error	Sergey Smolov	Alexander Kamkin	
9478	Retrascope RISC-V Benchmark	Bug	New	Normal	ERROR: retrascope-riscv\src\main\verilog\rocket-chip\src\main\resources\src\TestDriver.v line 28:2 no viable alternative at input 'int'	Sergey Smolov		
9482	Retrascope RISC-V Benchmark	Bug	Closed	Normal	ru.ispras.retrascope.sample.VexRiscvVexRiscvGaddTestCase: ERROR: Wrong number of out edges for 'ru.ispras.retrascope.model.cfg.CfgBlockStatement@c219bf5': 2	Sergey Smolov	Sergey Smolov	
9485	Retrascope	Bug	Closed	Normal	missing javadoc	Sergey Smolov	Mikhail Lebedev	1.0
9521	Retrascope	Bug	Closed	High	NuSMV works too slow on ITC'99 b11 design	Sergey Smolov	Mikhail Lebedev	1.0
9562	Retrascope	Bug	Closed	Normal	ru.ispras.retrascope.engine.hldd.printer.smv.undef.MemStageUseDefSmvPrinterTestCase: model checker crashes without errors in *.smvlog	Sergey Smolov	Mikhail Lebedev	1.0
9594	Verilog Translator	Bug	Closed	Normal	extra 'BVEXTRACT' operation in right hand side expression in 'assign' block's statement	Sergey Smolov	Alexander Kamkin	0.1
9763	Retrascope Test Suite	Bug	Closed	Normal	missing javadoc headers in Java files of 'ru.ispras.retrascope.engine.hldd.printer.smv.spec.sample.vcegar' package	Sergey Smolov	Mikhail Lebedev	
9773	Verilog Translator	Bug	Rejected	Normal	ru.ispras.verilog.parser.VerilogIeeeTestCase.runTest_10_04_03_1: ru.ispras.fortress.expression.NodeOperation cannot be cast to ru.ispras.fortress.expression.NodeValue	Sergey Smolov	Alexander Kamkin	0.1
9775	Verilog Translator	Bug	Closed	Normal	ru.ispras.verilog.parser.VerilogIeeeTestCase.runTest_10_04_04_1: Conversion = ""	Sergey Smolov	Alexander Kamkin	0.1
9784	Verilog Translator	Bug	Closed	Normal	mul_fifo.v: wrong Fortress-based node representation of assignment left-hand side	Sergey Smolov	Sergey Smolov	0.1
9798	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.sample.Bug9798TestCase: incorrect BVEXTRACT params for bit vector variable with offset	Sergey Smolov	Alexander Kamkin	0.1
9802	Verilog Translator	Bug	Closed	Normal	ru.ispras.verilog.parser.sample.FuncTestCase: NullPointerException at ru.ispras.verilog.parser.elaborator.VerilogElaborator.createVariableAndBinding(VerilogElaborator.java:512)	Sergey Smolov	Alexander Kamkin	0.1
9803	Verilog Translator	Bug	Closed	Normal	ru.ispras.verilog.parser.sample.MulFifoTestCase: NullPointerException at ru.ispras.verilog.parser.elaborator.VerilogElaborator\$1.getNode(VerilogElaborator.java:932)	Sergey Smolov	Alexander Kamkin	0.1
9816	Retrascope IDE	Bug	New	Normal	Retrascope IDE does not appear in "Installed Software" menu	Sergey Smolov		0.1

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9822	Verilog Translator	Bug	Closed	Normal	ru.ispras.verilog.parser.VerilogIeeeTestCase.runTest_10_04_04_1: Starting points limit has been exhausted: 513	Sergey Smolov	Sergey Smolov	0.1
9844	Retrascope Test Suite	Bug	Rejected	Normal	Bash scripts that run side tools (EBMC, SymbiYosys, Verilog2SMV) can't extract names of several Verilog modules	Sergey Smolov	Sergey Smolov	
9848	Verilog Translator	Bug	Closed	Normal	ru.ispras.verilog.parser.VerilogVisVerilog2SmvTestCase.runTest_Pci_Bus_Verilog_Mv_files_PciNorm: Function declaration '\$ND' has not been found	Sergey Smolov	Sergey Smolov	0.1
9892	MicroTESK for RISC-V	Bug	Closed	Normal	WARNING: An illegal reflective access operation has occurred	Sergey Smolov	Alexander Protsenko	0.1
9901	Retrascope Test Suite	Bug	New	Low	initializationError in some tests after Jenkins update	Sergey Smolov	Mikhail Lebedev	
9902	Verilog Translator	Bug	New	High	java.lang.IllegalArgumentException: Descriptor for '<var name>' has not been found	Sergey Smolov	Alexander Kamkin	0.1
9915	Verilog Translator	Bug	Closed	Urgent	"Cycle inclusion has been detected in fine <filename>" error is reported for Verilog modules that use the same another file	Sergey Smolov	Alexey Danilov	0.1
9936	Verilog Translator	Bug	Closed	High	tabs in ""define" directive cause java.lang.NumberFormatException	Sergey Smolov	Alexey Danilov	0.1
9962	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.sample.Mips16CoreTopTestCase: java.lang.IllegalArgumentException	Sergey Smolov	Alexey Danilov	0.1
9993	Verilog Translator	Bug	New	High	if two modules are passed to the tool and one includes another, the tool hangs	Sergey Smolov	Alexander Kamkin	0.1
10023	Retrascope	Bug	Closed	High	ru.ispras.retrascope.parser.verilog.VerilogParserTestCase: java.lang.Exception: Method runTest should have no parameters	Sergey Smolov	Maxim Chudnov	1.1
10031	MicroTESK for PowerPC	Bug	New	Normal	WARNING: An illegal reflective access operation has occurred	Sergey Smolov	Alexander Protsenko	0.0
10041	QEMU4V	Bug	Closed	Normal	wrong names for PowerPC registers in trace	Sergey Smolov	Sergey Smolov	0.3
10069	MicroTESK	Bug	New	Normal	cpu.nml Error: Internal error: context [/lisa] 1:8 attribute file isn't defined	Sergey Smolov	Alexander Kamkin	2.6
10075	Retrascope	Bug	Closed	Normal	jython.jar: WARNING: An illegal reflective access operation has occurred at JDK 11	Sergey Smolov	Sergey Smolov	1.1
10081	Retrascope	Bug	Closed	High	tool hangs right after final "Duration: " msg	Sergey Smolov	Sergey Smolov	1.1
10082	Retrascope	Bug	New	Normal	WARNING: Illegal reflective access by org.python.core.PySystemState	Sergey Smolov	Sergey Smolov	1.1
10085	Retrascope	Bug	Closed	Normal	E fsmTransitionPropertyExtractorTestCase: There is no declaration of variable neither in this EFSM nor in its ancestors: process_0.D	Sergey Smolov	Sergey Smolov	1.1
10094	MicroTESK	Bug	Closed	Normal	strange common code at LinkerScript.stg	Sergey Smolov	Alexander Kamkin	2.5
10102	MicroTESK	Bug	Closed	High	incorrect ld scripts for x86 test programs	Sergey Smolov	Alexander Kamkin	2.5
10121	MicroTESK	Bug	Open	Normal	technical output printing at 'compile.sh' script running with '--help' option	Sergey Smolov	Alexander Kamkin	2.6
10131	Verilog Translator	Bug	Closed	Normal	ru.ispras.verilog.parser.VerilogIwlsTestCase.runTest_iscas_s9234_1: java.lang.OutOfMemoryError: Java heap space	Sergey Smolov	Alexander Kamkin	0.1
10141	Verilog Translator	Bug	Closed	Normal	check port redeclarations	Sergey Smolov	Alexey Danilov	0.1

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10173	Verilog Translator	Bug	Closed	High	javadoc: DefineStructure.java:37: warning: no @return	Sergey Smolov	Alexey Danilov	0.1
10174	Retrascope	Bug	Closed	High	nondeterminism at EFSM transitions generation	Sergey Smolov	Sergey Smolov	1.1
10191	Retrascope	Bug	Closed	Normal	java.lang.IllegalArgumentException: Specified target vertex 0 is not part of graph	Sergey Smolov	Sergey Smolov	1.1
10202	Verilog Translator	Bug	Closed	Normal	SVA grammar warnings via assembling	Sergey Smolov	Mikhail Lebedev	0.1
10214	Verilog Translator	Bug	Rejected	Normal	ru.ispras.verilog.parser.VerilogQuipTestSuite#runTest_nut_000: nut_000_lut.v line 7:0 no viable alternative at input 'module'	Sergey Smolov	Sergey Smolov	0.1
10215	Verilog Translator	Bug	New	Normal	ERROR: Starting points limit has been exhausted: 2255	Sergey Smolov	Alexander Kamkin	0.1
10216	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.VerilogQuipTestSuite#runTest_nut_001: java.lang.NullPointerException	Sergey Smolov	Alexey Danilov	0.1
10236	Retrascope	Bug	Rejected	Normal	efsm-test-generator hangs at opencores/mips16/data_mem.v	Sergey Smolov	Sergey Smolov	1.1
10237	Verilog Translator	Bug	Closed	High	ru.ispras.verilog.parser.VerilogTexas97TestSuite#runTest_Pi_Bus_single_master_main2: ERROR: Cycle inclusion at: '...bus.v'	Sergey Smolov	Alexey Danilov	0.1
10241	Verilog Translator	Bug	Closed	Normal	ru.ispras.verilog.parser.VerilogQuipTestSuite#runTest_dctub_jpeg: ERROR: ..src\test\verilog\hdl-benchmarks\hdl\quip\oc_video_compression_systems_jpeg\dct_cos_table.v line 1:70 mismatched character 'r' expecting 'n'	Sergey Smolov	Alexander Kamkin	0.1
10245	Verilog Translator	Bug	Closed	Normal	ru.ispras.verilog.parser.VerilogQuipTestSuite#runTest_pci_wbw_wbr_fifos: ERROR: [Internal] null	Sergey Smolov	Alexey Danilov	0.1
10246	Verilog Translator	Bug	Rejected	Normal	ru.ispras.verilog.parser.VerilogQuipTestSuite#runTest_nut_001: ERROR: Module 'lut_output' has not been found	Sergey Smolov	Alexander Kamkin	0.1
10266	Retrascope	Bug	Closed	Normal	ru.ispras.retrascope.engine.hidd.printer.smv.HiddSmvPrinterTestCase.runTest: java.lang.NullPointerException	Sergey Smolov	Mikhail Lebedev	1.1
10289	Retrascope	Bug	Closed	Normal	ru.ispras.retrascope.engine.hidd.printer.smv.property.HiddPropertySmvPrinterTestCase.runTest: java.lang.OutOfMemoryError: Java heap space	Sergey Smolov	Mikhail Lebedev	1.1
10370	Fortress	Bug	Closed	Normal	class ru.ispras.fortress.solver.constraint.Formulas cannot be cast to class ru.ispras.fortress.solver.constraint.Sat4jFormula	Sergey Smolov	Sergey Smolov	0.4
10382	Verilog Translator	Bug	Closed	Normal	java.lang.IllegalArgumentException: expression=(BVREPEAT test.uut._saxi_maskwidth 1)	Sergey Smolov	Sergey Smolov	0.1
10502	Verilog Translator	Bug	New	Normal	subbytes.v line 76:13 no viable alternative at input '['	Sergey Smolov	Alexander Kamkin	0.1
10505	Verilog Translator	Bug	New	Normal	ERROR: [Internal] 11 must be within range [0, 1)	Sergey Smolov	Alexander Kamkin	0.1
10508	Verilog Translator	Bug	New	Normal	ERROR: [Internal] Java heap space	Sergey Smolov	Alexander Kamkin	0.1
10509	Verilog Translator	Bug	New	Normal	ERROR: [Internal] 0 must be > 0	Sergey Smolov	Alexander Kamkin	0.1

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10510	Verilog Translator	Bug	New	Normal	ERROR: [Internal] Bit vector sizes do not match: 32 != 2.	Sergey Smolov	Alexander Kamkin	0.1
10512	Verilog Translator	Bug	New	Normal	ADDA162H90A_atop.v line 120:47 mismatched input ':' expecting RPAREN	Sergey Smolov	Alexander Kamkin	0.1
10513	Verilog Translator	Bug	New	Normal	macOS related line endings at Verilog modules	Sergey Smolov	Alexander Kamkin	0.1
10819	MicroTESK for PowerPC	Bug	New	Normal	Trace Matcher crashes on QEMU4V empty trace	Sergey Smolov	Sergey Smolov	
11042	Java SoftFloat	Bug	New	Normal	Javadoc warnings	Sergey Smolov	Alexander Protsenko	2.0
12249	MicroTESK for PowerPC	Bug	New	Normal	qemu-system-ppc: failed to find romfile "efi-virtio.rom"	Sergey Smolov	Sergey Smolov	
12607	QEMU4V	Bug	New	Normal	missing log problem	Sergey Smolov	Sergey Smolov	
8197	Trace Matcher	Feature	Closed	Normal	"matching window in ticks" command line option	Sergey Smolov	Sergey Smolov	0.1
8198	Trace Matcher	Feature	Closed	Normal	"exit-on-first-divergence" command line option	Sergey Smolov	Sergey Smolov	0.1
8199	Trace Matcher	Feature	Closed	Normal	"ignore-the-rest" command line option	Sergey Smolov	Sergey Smolov	0.1
8203	Fortress	Feature	Closed	Normal	bv2nat\int2bv operations	Sergey Smolov	Sergey Smolov	0.4
8204	Fortress	Feature	Closed	Normal	solver-specific header for generated SMT2 files	Sergey Smolov	Sergey Smolov	0.4
8206	Trace Matcher	Feature	Closed	Normal	"--debug" command line option	Sergey Smolov	Sergey Smolov	0.1
8220	Retrascope	Feature	Closed	Normal	BV_INC6 VHDL function support	Sergey Smolov	Sergey Smolov	0.2
8260	Retrascope	Feature	Closed	Normal	VHDL record support (non-aggregate case)	Sergey Smolov	Maxim Chudnov	1.0
8262	Retrascope	Feature	Closed	Normal	phase variable based approach for CFG-CGAA-EFSM optimisation	Sergey Smolov	Sergey Smolov	0.2
8282	Retrascope	Feature	Closed	Normal	apply SLV detection heuristic to more than one CGAA path	Sergey Smolov	Sergey Smolov	0.2
8304	Retrascope	Feature	Rejected	Normal	SLR values number limit	Sergey Smolov	Sergey Smolov	0.2
8305	Retrascope	Feature	Closed	Normal	EFSM state limit	Sergey Smolov	Sergey Smolov	0.2
8433	Trace Matcher	Feature	Closed	Normal	"--skip-equal" command line option	Sergey Smolov	Sergey Smolov	0.1
8587	MicroTESK	Feature	New	Normal	ISA subsets	Sergey Smolov	Artem Kotsynyak	2.6
8615	Retrascope	Feature	Closed	Normal	"--no-backends" command line option	Sergey Smolov	Sergey Smolov	1.0
8665	Fortress	Feature	Closed	High	Nodes.BVEXTRACT(Node, Node, Node) convenience method	Sergey Smolov	Andrei Tatarnikov	0.4
8667	Fortress	Feature	Closed	Normal	Nodes.EQ(Node ... nodes) convenience method	Sergey Smolov	Andrei Tatarnikov	0.4
8702	Fortress	Feature	Closed	Normal	'public static NodeValue.newBitVector(final boolean value)' convenience method	Sergey Smolov	Andrei Tatarnikov	0.4
8703	Fortress	Feature	Closed	Normal	'public static boolean isType(final Node node, final DataType ... types)' convenience method	Sergey Smolov	Andrei Tatarnikov	0.4
8709	Fortress	Feature	Closed	Normal	'public static boolean isOperation(final Node node, final T ... opTypes)' convenience method	Sergey Smolov	Andrei Tatarnikov	0.4
8866	QEMU4V	Feature	Closed	Normal	trace generation for MIPS programs	Sergey Smolov	Maxim Chudnov	0.2

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8867	QEMU4V	Feature	Closed	Normal	trace generation for PowerPC (32bit) programs	Sergey Smolov	Maxim Chudnov	0.3
8868	QEMU4V	Feature	Closed	Normal	implement tracer that is activated by "-trace-log" command line option	Sergey Smolov	Sergey Smolov	
8869	QEMU4V	Feature	Closed	Normal	trace generation for Aarch64 programs	Sergey Smolov	Sergey Smolov	
8870	QEMU4V	Feature	Closed	Normal	trace generation for RISC-V programs	Sergey Smolov	Sergey Smolov	
8871	QEMU4V	Feature	Closed	Normal	"-print-pte-addr" cmdline option	Sergey Smolov	Sergey Smolov	
8874	Verilog Translator	Feature	Closed	High	mapping from instance variables to their code entries	Sergey Smolov	Alexander Kamkin	0.1
9039	Retrascope	Feature	Closed	Normal	Support for designs that assign to variable more than once	Sergey Smolov	Sergey Smolov	1.0
9041	Retrascope	Feature	Closed	Normal	when model checker returns an error, print it's log to the Retrascope output	Sergey Smolov	Mikhail Lebedev	1.0
9049	QEMU4V	Feature	Closed	Normal	basic support for MIPS64 emulation	Sergey Smolov	Sergey Smolov	0.2
9050	QEMU4V	Feature	Closed	Normal	basic support for i386 emulation	Sergey Smolov	Sergey Smolov	
9051	QEMU4V	Feature	Closed	Normal	basic support for PowerPC emulation	Sergey Smolov	Sergey Smolov	0.3
9079	QEMU4V	Feature	Closed	Normal	basic support for MIPS32	Sergey Smolov	Sergey Smolov	0.2
9123	Fortress	Feature	Closed	High	calculate DataType for 'BVEXTRACT(i, i, x)' NodeOperation objects	Sergey Smolov	Sergey Smolov	0.4
9149	Retrascope	Feature	Closed	Normal	elaborate ranged assignments for bitvector target variables	Sergey Smolov	Sergey Smolov	1.0
9227	Retrascope	Feature	Closed	High	support for 'BVEXTRACT(x y (SELECT z w))' constructions in left hand sides of assignments	Sergey Smolov	Sergey Smolov	1.0
9247	Retrascope	Feature	Open	High	CFG-to-C printer	Sergey Smolov	Sergey Smolov	1.2
9264	Retrascope	Feature	Closed	Normal	'--disable-backends' cmdline option for HDL parser engine	Sergey Smolov	Sergey Smolov	1.0
9281	Retrascope	Feature	Closed	Normal	cmdline option that specifies clock variable for CGAA model	Sergey Smolov	Sergey Smolov	1.0
9335	Retrascope	Feature	Closed	Normal	cgaa-assert-extractor engine	Sergey Smolov	Mikhail Lebedev	1.0
9446	Retrascope	Feature	Closed	Normal	Debug output file for engines and their backends	Sergey Smolov	Sergey Smolov	1.0
9457	Retrascope	Feature	Closed	Normal	one more auxiliary path in GADD model for terminal endings	Sergey Smolov	Sergey Smolov	1.0
9468	Retrascope	Feature	Closed	Normal	HDL parser backend that removes 'initial' processes	Sergey Smolov	Sergey Smolov	1.0
9474	Retrascope	Feature	Closed	Normal	enable/disable backend parameters for all the engines	Sergey Smolov	Sergey Smolov	1.0
9486	Retrascope	Feature	Closed	Normal	HDL parser's init_process backend: calculate initial values if possible	Sergey Smolov	Sergey Smolov	1.0
9503	Retrascope	Feature	Closed	Normal	when debug option is enabled, pass it to the model checker as well	Sergey Smolov	Mikhail Lebedev	1.0
9767	Retrascope	Feature	Closed	Normal	GraphML printers: use dotted arrows for Module->(Module Process) hierarchy dependencies	Sergey Smolov	Sergey Smolov	1.0
9769	Retrascope	Feature	Closed	Normal	GraphML printers: make branch values italic	Sergey Smolov	Sergey Smolov	1.0
9990	Verilog Translator	Feature	Closed	High	check for variable/net redeclarations	Sergey Smolov	Alexey Danilov	0.1
10015	Trace Matcher	Feature	Closed	Normal	Report an error when input file is empty	Sergey Smolov	Sergey Smolov	0.1
10060	Retrascope	Feature	Closed	High	Support SVA properties in CFG model	Sergey Smolov	Sergey Smolov	1.2
10074	MicroTESK	Feature	New	Normal	option that stores boot obj at the generated ld script	Sergey Smolov	Alexander Kamkin	2.6

#	Project	Tracker	Status	Priority	Subject	Author	Assignee	Target version
10088	QEMU4V	Feature	New	Low	QEMU4V formatted traces for x86 programs	Sergey Smolov		
10099	Trace Matcher	Feature	Resolved	Normal	"--start-addr <hex value>" command line option	Sergey Smolov	Sergey Smolov	0.1
10100	Trace Matcher	Feature	Resolved	Normal	"--boot-size <num>" command line option	Sergey Smolov	Sergey Smolov	0.1
10112	Retrascope	Feature	Closed	Normal	'--no-phase' command line option for 'cfg-gadd-transformer' engine	Sergey Smolov	Sergey Smolov	1.1
10115	Retrascope	Feature	Closed	Normal	'--version' command line option	Sergey Smolov	Sergey Smolov	1.1
10116	Retrascope	Feature	Closed	Normal	command line option to check if solvers/model checkers that are used are installed properly	Sergey Smolov	Sergey Smolov	1.1
10125	Retrascope	Feature	Closed	Normal	'--detailed' option for efsm-graphml-printer engine	Sergey Smolov	Sergey Smolov	1.1
10238	Retrascope	Feature	Closed	Normal	VerilogParser: '--library-file' cmdline option	Sergey Smolov	Sergey Smolov	1.1
10287	Retrascope	Feature	Closed	Normal	TestModel: keep top level module name & variables	Sergey Smolov	Sergey Smolov	1.1
10290	Verilog Translator	Feature	New	Normal	SystemVerilog support	Sergey Smolov		
3979	Retrascope	Developer Request	Closed	Normal	Реструктурирование проекта	Sergey Smolov	Sergey Smolov	
5580	Retrascope	Developer Request	Closed	Normal	[efsm][conflict][extractor][jaxb] can GuardedAction() call at the JaxbGuardedActionAdapter be substituted by something else	Sergey Smolov	Mikhail Lebedev	0.1
6537	Retrascope	Developer Request	Closed	Normal	Efsm: collection of resetting guarded actions	Sergey Smolov	Igor Melnichenko	0.1
12038	MicroTESK for Plasma	Developer Request	Resolved	Normal	обновление плагина PMD в Gradle	Sergey Smolov	Alexander Protsenko	
2224	C++TESK Development Environment	Task	Closed	Normal	Добавить пункт со сведениями о плагине	Sergey Smolov	Alexander Kamkin	
3406	Retrascope	Task	Closed	Normal	CFG extraction from guarded atomic actions (GAA) set.	Sergey Smolov	Sergey Smolov	
3434	Retrascope	Task	Closed	Normal	Извлечение "протоопераций" из Data Flow Graph	Sergey Smolov	Sergey Smolov	
3623	C++TESK Development Environment	Task	Closed	Normal	Внутреннее представление для прототипов тестовых систем	Sergey Smolov	Sergey Smolov	
3624	C++TESK Development Environment	Task	Closed	Normal	XML dumping/parsing	Sergey Smolov	Sergey Smolov	
3637	Retrascope	Task	Closed	Normal	Пространство состояний	Sergey Smolov	Sergey Smolov	
3654	C++TESK Development Environment	Task	Closed	High	source code refactoring	Sergey Smolov	Sergey Smolov	
3659	C++TESK Development Environment	Task	New	Normal	Соответствие полей классов сообщений и сигналов HDL-модели	Sergey Smolov		
3694	Fortress	Task	Closed	Normal	Операции сравнения битовых векторов	Sergey Smolov	Andrei Tatarnikov	

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3708	Fortress	Task	Closed	Normal	Методы makeNegation, makeConjunction, makeDisjunction класса Constraint	Sergey Smolov	Sergey Smolov	
3716	C++TESK Development Environment	Task	Closed	Normal	Simple XML dumping\parsing test	Sergey Smolov	asd ert	
3721	Fortress	Task	Closed	Normal	Дополнительные операции	Sergey Smolov	Sergey Smolov	
3734	Fortress	Task	Closed	Normal	Операции сравнения для LOGIC-типов	Sergey Smolov	Sergey Smolov	
3754	C++TESK Development Environment	Task	Closed	Normal	флаг incomparable в полях сообщений	Sergey Smolov	Sergey Smolov	
3755	C++TESK Development Environment	Task	New	Normal	namespace name for test system prototypes	Sergey Smolov		
3756	C++TESK Development Environment	Task	New	Immediate	Генерация C++ кода для модели сообщений	Sergey Smolov		
3759	C++TESK Development Environment	Task	Feedback	Normal	Разработать демонстрационный пример для структуры соответствия	Sergey Smolov		
3895	Fortress	Task	Closed	Normal	Дополнительные операции Verilog	Sergey Smolov	Sergey Smolov	
3914	Fortress	Task	Rejected	Normal	function templates	Sergey Smolov	Andrei Tatarnikov	0.1
3934	Retrascope	Task	Closed	Normal	Дополнительные операции	Sergey Smolov	Sergey Smolov	
3950	Retrascope	Task	Closed	Normal	Переместить служебные файлы Eclipse	Sergey Smolov	Igor Melnichenko	
3957	Retrascope	Task	Closed	High	DFG to EFSM	Sergey Smolov	Sergey Smolov	
3973	Fortress	Task	Closed	Normal	Реализовать добавление Variable в Constraint	Sergey Smolov	Sergey Smolov	0.1
4133	Fortress	Task	Closed	Normal	ABS, MAX, MIN для Logic-типов	Sergey Smolov	Sergey Smolov	0.1
4175	Fortress	Task	Closed	Normal	Добавить параметризованные операции	Sergey Smolov	Sergey Smolov	0.1
4337	Retrascope	Task	Closed	Normal	реализовать заглушки для методов преобразования в ограничения	Sergey Smolov	Sergey Smolov	
4359	Retrascope	Task	Rejected	Normal	[cfg] Реализовать метод toConstraint()	Sergey Smolov	Igor Melnichenko	0.1
4363	Retrascope	Task	New	Low	Критерий кластеризации входных сигналов, основанный на GA	Sergey Smolov	Sergey Smolov	2.0
4465	Retrascope	Task	Closed	Normal	Объединение присваиваний в базовых блоках	Sergey Smolov	Sergey Smolov	
4466	Retrascope	Task	Closed	Normal	[vhdl][parser][cfg] преобразование IGSequentialWait	Sergey Smolov	Sergey Smolov	0.2
4521	Retrascope	Task	New	Low	Входной класс для генератора тестовой последовательности	Sergey Smolov	Sergey Smolov	2.0
4554	Fortress	Task	Closed	Normal	[solver][xml] Метод преобразования ограничения в XML-based String	Sergey Smolov	Andrei Tatarnikov	0.3
4558	Retrascope	Task	Closed	Normal	[cfg][model] Реализовать обходчик для внутреннего представления описаний аппаратуры	Sergey Smolov	Sergey Smolov	0.1
4580	Retrascope	Task	Closed	Normal	Поместить проект MiniMIPS в share/vhdl	Sergey Smolov	Sergey Smolov	

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4671	Fortress	Task	Closed	Normal	[data] Метод построения битовых векторов из их строкового представления	Sergey Smolov	Sergey Smolov	0.3
4673	Fortress	Task	Closed	Normal	[solver][constraint] Ограничения без имен	Sergey Smolov	Sergey Smolov	0.3
4674	TestBase	Task	New	Normal	Тестовые ситуации	Sergey Smolov	Artem Kotsynyak	0.0
4699	Fortress	Task	Closed	Normal	[data][solver] поддержка массивов SMT-LIB	Sergey Smolov	Andrei Tatarnikov	0.3
4702	Fortress	Task	Closed	Normal	[expression] Реализовать операцию BVBIT	Sergey Smolov	Alexander Kamkin	0.3
4713	Fortress	Task	New	High	SMT-LIB structures	Sergey Smolov	Artem Kotsynyak	0.4
4802	Fortress	Task	Closed	Normal	[solver][constraint] создание Constraint без указания variables	Sergey Smolov	Andrei Tatarnikov	0.3
4807	Retrascope	Task	Closed	Normal	Action as interface for BasicBlock, Assertion, Situation	Sergey Smolov	Sergey Smolov	
4829	Retrascope	Task	Closed	Normal	[cfg][transformer][cгаа] CFG: Assertion building	Sergey Smolov	Sergey Smolov	0.1
4924	Retrascope	Task	Closed	Normal	[cfg][model] Представление непрерывных присваиваний	Sergey Smolov	Sergey Smolov	0.1
4925	Retrascope	Task	Closed	Normal	[vhd][translator] Обработка непрерывных присваиваний	Sergey Smolov	Sergey Smolov	0.1
4927	Retrascope	Task	Rejected	Normal	[cfg][model] Убрать узел типа ASSERT	Sergey Smolov	Sergey Smolov	0.1
4929	Retrascope	Task	Rejected	Normal	[cfg][model] Добавить структуру данных для представления задержек (delay) в присваиваниях	Sergey Smolov	Sergey Smolov	0.2
4945	Retrascope	Task	Closed	Normal	[basis][log] Опция логирования	Sergey Smolov	Alexander Kamkin	0.1
4946	Retrascope	Task	Closed	Normal	[basis][log] Ведение лога для нескольких логгеров	Sergey Smolov	Alexander Kamkin	0.1
4966	Retrascope	Task	Closed	Normal	[model][basis] Убрать поле isDefined класса MVariableData	Sergey Smolov	Sergey Smolov	0.1
4967	Retrascope	Task	Closed	Normal	[model][basis] Реализовать хранилище деклараций переменных	Sergey Smolov	Sergey Smolov	0.1
4971	Retrascope	Task	Rejected	Normal	[model][basis] AssignAtomicStatement vs Binding	Sergey Smolov	Sergey Smolov	0.1
4972	Retrascope	Task	Closed	Normal	[model][cгаа] странное расположение метода addVarNamePrefix	Sergey Smolov	Sergey Smolov	0.1
4984	Retrascope	Task	Closed	Normal	[vhd][translator] Группировка неблокирующих присваиваний	Sergey Smolov	Sergey Smolov	0.1
4998	Retrascope	Task	Closed	Normal	[model][cгаа] Data structure for guarded actions decision diagram	Sergey Smolov	Sergey Smolov	0.1
4999	Retrascope	Task	Closed	Normal	[cfg][transformer][cгаа] CFG-to-GADD transformer	Sergey Smolov	Sergey Smolov	0.1
5090	Retrascope	Task	Closed	Normal	[cfg] Оптимизация представления ветвлений	Sergey Smolov	Sergey Smolov	0.1
5095	Retrascope	Task	Closed	Normal	[parser][cfg] Оптимизация представления ветвлений - многовариантные узлы switch	Sergey Smolov	Sergey Smolov	0.1
5107	Retrascope	Task	Closed	Normal	[cfg] Реализовать VhdlExpressionPrinter	Sergey Smolov	Sergey Smolov	0.1
5108	Retrascope	Task	Closed	Normal	[parser] Реализовать базовые классы Parser, Frontend, Backend	Sergey Smolov	Sergey Smolov	0.1
5116	Retrascope	Task	Closed	Normal	[parser][basis][backend] CfgBasicBlockBackend	Sergey Smolov	Sergey Smolov	0.1
5117	Retrascope	Task	Closed	Normal	[parser][basis][backend] CfgMergeBackend	Sergey Smolov	Sergey Smolov	0.1
5122	Retrascope	Task	Closed	Normal	[parser][backend] elaborate non-blocking assignments	Sergey Smolov	Sergey Smolov	0.2
5127	Retrascope IDE	Task	Rejected	Normal	[cfg][printer][graphml] Интегрировать плагин для уEd	Sergey Smolov	Alexander Protsenko	
5142	Retrascope	Task	Closed	Normal	[wiki] Классификация Engine	Sergey Smolov	Sergey Smolov	0.1

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5143	Retrascope	Task	Closed	Normal	[cfg][extractor][iface] CfgIfaceExtractor	Sergey Smolov	Sergey Smolov	0.1
5145	Retrascope	Task	Closed	Normal	[testbench] Iface	Sergey Smolov	Sergey Smolov	0.1
5157	Retrascope	Task	Closed	Normal	[cfg] addNewVariable(DataType type)	Sergey Smolov	Sergey Smolov	0.1
5161	Retrascope	Task	Closed	Normal	[parser][cfg] Обработка циклов	Sergey Smolov	Sergey Smolov	0.2
5175	Retrascope	Task	Closed	Normal	[vhdl][parser] IG array elaboration	Sergey Smolov	Sergey Smolov	0.2
5226	Retrascope	Task	Closed	Normal	[cfg][printer][graphml] Узлы SOURCE и BASIC_BLOCK имеют одинаковый цвет	Sergey Smolov	Sergey Smolov	0.1
5229	Fortress	Task	Closed	High	[transformer] Упрощение выражений с LOGIC_BOOLEAN	Sergey Smolov	Artem Kotsynyak	0.3
5247	Retrascope	Task	Closed	Normal	[basis] Набор идентификаторов Engine как опция командной строки Retrascope	Sergey Smolov	Alexander Kamkin	0.1
5249	Retrascope	Task	Closed	High	[basis] Настройка Retrascope для работы с SMT-решателями	Sergey Smolov	Alexander Kamkin	0.1
5251	Retrascope IDE	Task	New	Normal	[tool][configurator] Сохранение конфигураций	Sergey Smolov		0.1
5258	Retrascope	Task	Closed	High	[basis] Обработка циклических зависимостей разных Engine	Sergey Smolov	Alexander Kamkin	0.1
5259	Fortress	Task	Rejected	Normal	[build] удаление папки distr при выполнении команды ant clean	Sergey Smolov	Andrei Tatarnikov	0.3
5313	Fortress	Task	Closed	Normal	[expression] Сделать публичным метод ExprUtils.isSAT(Node assertion)	Sergey Smolov	Andrei Tatarnikov	0.3
5316	Fortress	Task	Closed	Low	[expression] Операции теории множеств над коллекциями объектов Node	Sergey Smolov	Andrei Tatarnikov	0.3
5317	Fortress	Task	Closed	Low	[expression] Реализовать метод построения Constraint по Node	Sergey Smolov	Andrei Tatarnikov	0.3
5318	Fortress	Task	Closed	Low	[solver][expression] Реализовать метод разрешения ограничений SolverResult solve(Constraint constraint)	Sergey Smolov	Andrei Tatarnikov	0.3
5319	Fortress	Task	Closed	Low	[expression] Реализовать метод получения коллекции NodeVariable по объекту Node	Sergey Smolov	Andrei Tatarnikov	0.3
5320	Retrascope	Task	Rejected	Normal	[cfg] Методы копирования вершин CFG	Sergey Smolov	Sergey Smolov	0.2
5322	Retrascope	Task	Closed	Normal	[cгаа][transformer][efsm] Продумать и реализовать эвристику определения reset	Sergey Smolov	Sergey Smolov	0.2
5394	Retrascope	Task	Closed	High	[cгаа][transformer][efsm] реализовать построение переходов EFSM	Sergey Smolov	Sergey Smolov	0.1
5395	Retrascope	Task	Closed	Normal	[cfg] getOnlyChild(), getOnlyParent()	Sergey Smolov	Sergey Smolov	0.2
5398	Retrascope	Task	Closed	Normal	[verilog][parser][cfg] Преобразование констант в NodeValue	Sergey Smolov	Mikhail Chupilko	0.1
5399	Fortress	Task	Closed	Normal	silent & debug mode	Sergey Smolov	Andrei Tatarnikov	0.3
5413	Retrascope	Task	Closed	High	[model][basis] add HdIType field to VariableData class	Sergey Smolov	Sergey Smolov	0.1
5416	Retrascope	Task	Closed	Normal	[model][basis] мета-информация	Sergey Smolov	Sergey Smolov	0.1
5419	Fortress	Task	Closed	High	[transformer][ruleset] реализовать правило expr==false -> NOT(expr == true)	Sergey Smolov	Artem Kotsynyak	0.3
5420	Retrascope	Task	Closed	Normal	[util] метод fillNodeWithValues заменить на Transformer.substituteAllBindings	Sergey Smolov	Igor Melnichenko	0.1
5424	Fortress	Task	Closed	High	[transformer][ruleset] дополнительные правила стандартизации	Sergey Smolov	Artem Kotsynyak	0.3
5433	Fortress	Task	Closed	Normal	[test] write executable SMT-LIB code at testcase comments	Sergey Smolov	Artem Kotsynyak	0.3
5446	Retrascope	Task	Closed	Normal	[efsm][examples] Добавить мета-информацию в B04/B13	Sergey Smolov	Sergey Smolov	0.1
5447	Fortress	Task	Closed	High	[transformer][ruleset] стандартизация константных выражений вида "x EQ y"	Sergey Smolov	Artem Kotsynyak	0.3

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5455	Verilog Translator	Task	Closed	Normal	устранить зависимость от ANTLRWorks	Sergey Smolov	Alexander Kamkin	0.1
5456	Retrascope	Task	Closed	Normal	[structure] Замечания по структуре каталогов	Sergey Smolov	Igor Melnichenko	0.1
5459	Retrascope	Task	Closed	Normal	implement EngineFrontend/EngineBackend	Sergey Smolov	Sergey Smolov	0.1
5462	Fortress	Task	Closed	Normal	[arrays] arrays initialization is inconvenient	Sergey Smolov	Artem Kotsynyak	0.3
5464	Fortress	Task	Closed	High	[solver] boolean expressions casting into bit vectors	Sergey Smolov	Andrei Tatarnikov	0.3
5465	Fortress	Task	Closed	Normal	[z3][solver] solver errors elaboration scheme	Sergey Smolov	Andrei Tatarnikov	0.3
5466	Fortress	Task	Closed	High	[solver] print the input constraint when solver returns ERROR/UNKNOWN verdict	Sergey Smolov	Andrei Tatarnikov	0.3
5471	Retrascope	Task	Closed	Normal	[structure] Rename *ing packages	Sergey Smolov	Igor Melnichenko	0.1
5478	Fortress	Task	Closed	Normal	Implement Transformer.reduce(Node expression)	Sergey Smolov	Artem Kotsynyak	0.4
5481	Retrascope	Task	Closed	Normal	[structure] remove raw packages from main build folder	Sergey Smolov	Sergey Smolov	0.1
5482	Retrascope	Task	Closed	Normal	[wiki] documentation for 0.1-alpha	Sergey Smolov	Sergey Smolov	0.1
5494	Retrascope	Task	Closed	Normal	[structure] remove ru.ispras.retrascope.engine.efsm.testgen.heuristic empty package	Sergey Smolov	Igor Melnichenko	0.1
5495	Retrascope	Task	Closed	Normal	[structure] move ru.ispras.retrascope.testbench.media package to ru.ispras.retrascope.result.testbench	Sergey Smolov	Igor Melnichenko	0.1
5497	Retrascope	Task	Closed	Normal	[efsm][extractor][conflict][jxb] rename jaxb-classes	Sergey Smolov	Mikhail Lebedev	0.1
5498	Retrascope	Task	Closed	Normal	[model][basis][memory] rename IMemory interface	Sergey Smolov	Igor Melnichenko	0.1
5501	Retrascope	Task	Closed	Normal	[efsm][generator][test] Class 'EfsmAtomicTestGenerator' is never used	Sergey Smolov	Igor Melnichenko	0.1
5503	Retrascope	Task	Closed	Normal	[parser][basis][backend] implement "atomic hammock" backend	Sergey Smolov	Sergey Smolov	0.1
5504	Retrascope	Task	New	Normal	add channels between EFSMs	Sergey Smolov	Mikhail Lebedev	1.2
5507	Retrascope	Task	Rejected	Normal	[engine][basis] implement PrinterEngine	Sergey Smolov	Sergey Smolov	0.1
5526	Retrascope	Task	Rejected	Normal	Retrascope engines configuration	Sergey Smolov	Alexander Kamkin	
5537	Retrascope	Task	Closed	Normal	[efsm][generator][test] make log shorter	Sergey Smolov	Igor Melnichenko	0.1
5541	Retrascope	Task	Closed	High	[engine][printer][smv] move engine.printer.smv package to sandbox	Sergey Smolov	Mikhail Lebedev	0.1
5546	Retrascope IDE	Task	New	Normal	[log] print Retrascope log to Eclipse log	Sergey Smolov		0.1
5548	Retrascope	Task	Closed	Low	elaborate minimips modules	Sergey Smolov	Sergey Smolov	0.2
5549	Retrascope	Task	Closed	Normal	[vhdl][cfg][parser] add support of instantiation	Sergey Smolov	Sergey Smolov	0.2
5561	Retrascope	Task	Closed	Normal	[project] use InvariantChecks if needed	Sergey Smolov	Sergey Smolov	0.1
5563	Fortress	Task	Closed	Normal	[data] implement DataTypeId.isLogic(Enum<?> id) method	Sergey Smolov	Andrei Tatarnikov	0.3
5568	Retrascope	Task	Closed	Normal	[cfg] support process variable declarations	Sergey Smolov	Sergey Smolov	0.1
5569	Retrascope	Task	Closed	Normal	support process variable declarations	Sergey Smolov	Sergey Smolov	0.1
5570	Retrascope	Task	Closed	Low	[build] build.xml: extract equal code parts from 'test'/test.short' targets	Sergey Smolov	Sergey Smolov	0.1
5576	Fortress	Task	Closed	Normal	Calculate data type of expression with BVCONCAT	Sergey Smolov	Andrei Tatarnikov	0.3

#	Project	Tracker	Status	Priority	Subject	Author	Assignee	Target version
5578	Retrascope	Task	Closed	Normal	[verilog][parser][cfg] add support of multiple assignments	Sergey Smolov	Mikhail Chupilko	0.1
5579	Retrascope	Task	Closed	Normal	[cfg] simplify the Assignment class	Sergey Smolov	Sergey Smolov	0.1
5588	Retrascope	Task	Closed	Normal	extend HDL test suite	Sergey Smolov	Sergey Smolov	1.0
5589	Retrascope	Task	Closed	Normal	[efsm][extraction] state-like variables use/def statistics	Sergey Smolov	Sergey Smolov	0.1
5590	Retrascope	Task	Closed	Normal	[efsm][extraction] implement an EFSM initial state & 'reset' signal heuristics	Sergey Smolov	Sergey Smolov	0.1
5591	Retrascope	Task	Closed	Normal	[project] run scripts for Unix/Windows	Sergey Smolov	Sergey Smolov	0.1
5592	Retrascope	Task	Closed	Normal	[project] prepare tar.gz distribution for future release	Sergey Smolov	Sergey Smolov	0.1
5599	Fortress	Task	Closed	Normal	[expression] implement getDataTypeId() method	Sergey Smolov	Andrei Tatarnikov	0.3
5600	Fortress	Task	Closed	High	[transformer][ruleset] implement ITE rules	Sergey Smolov	Artem Kotsynyak	0.3
5609	Retrascope	Task	Rejected	Normal	make process-local variables be efsm-model-global	Sergey Smolov	Sergey Smolov	0.1
5651	Verilog Translator	Task	Closed	Normal	Translate logic operation results into Boolean expressions	Sergey Smolov	Sergey Smolov	0.1
5683	Retrascope	Task	Closed	Normal	STD_LOGIC/STD_ULOGIC processing	Sergey Smolov	Sergey Smolov	0.1
5688	Retrascope	Task	Closed	Normal	implement test-to-VHDL printer	Sergey Smolov	Igor Melnichenko	0.1
5689	Retrascope	Task	Closed	High	implement test-to-Verilog printer	Sergey Smolov	Sergey Smolov	0.2
5694	Retrascope	Task	Closed	Normal	collect the *.smt2 files and analyse constraints	Sergey Smolov	Sergey Smolov	0.1
5695	Retrascope	Task	Closed	Normal	mark retrascope.sh as executable automatically	Sergey Smolov	Sergey Smolov	0.1
5696	Retrascope	Task	Closed	Normal	exclude sandbox & test folder from distribution	Sergey Smolov	Sergey Smolov	0.1
5702	Retrascope IDE	Task	New	Normal	[tool] create Retrascope icon	Sergey Smolov		0.1
5704	Retrascope	Task	Closed	Normal	try to find a way to remove 'toplevel' option	Sergey Smolov	Sergey Smolov	0.1
5711	Retrascope	Task	Closed	Normal	Check generated *.smv files with external model checker	Sergey Smolov	Mikhail Lebedev	1.0
5755	Retrascope	Task	Closed	Low	use Zamia IG visitors & walkers	Sergey Smolov	Sergey Smolov	0.1
5756	Retrascope	Task	Closed	Normal	EFSM pre-initial state + initialization action	Sergey Smolov	Sergey Smolov	0.1
5802	Fortress	Task	Closed	High	NodeValue newZero(DataType dataType)	Sergey Smolov	Andrei Tatarnikov	0.3
5832	Retrascope	Task	Closed	Normal	print some info about failed tests	Sergey Smolov	Sergey Smolov	0.1
5861	Fortress	Task	Closed	Low	static boolean containsSingleObject(Collection<?> collection)	Sergey Smolov	Andrei Tatarnikov	0.3
5868	Retrascope	Task	Closed	Normal	Migrate to Fortress 0.4	Sergey Smolov	Sergey Smolov	0.1
5870	Retrascope	Task	Closed	Normal	Retrascope exceptions	Sergey Smolov	Igor Melnichenko	0.1
5872	Retrascope	Task	Closed	Normal	HDL file meta info	Sergey Smolov	Sergey Smolov	0.1
5875	Retrascope	Task	Closed	Normal	Check state/transition count for extracted EFSM models	Sergey Smolov	Sergey Smolov	0.1

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